Oeabt
Optics Experiment and Basic Teaching

科学相机
130 万像素 FPGA+硬件缓存
全局快门近红外增强型

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科学相机

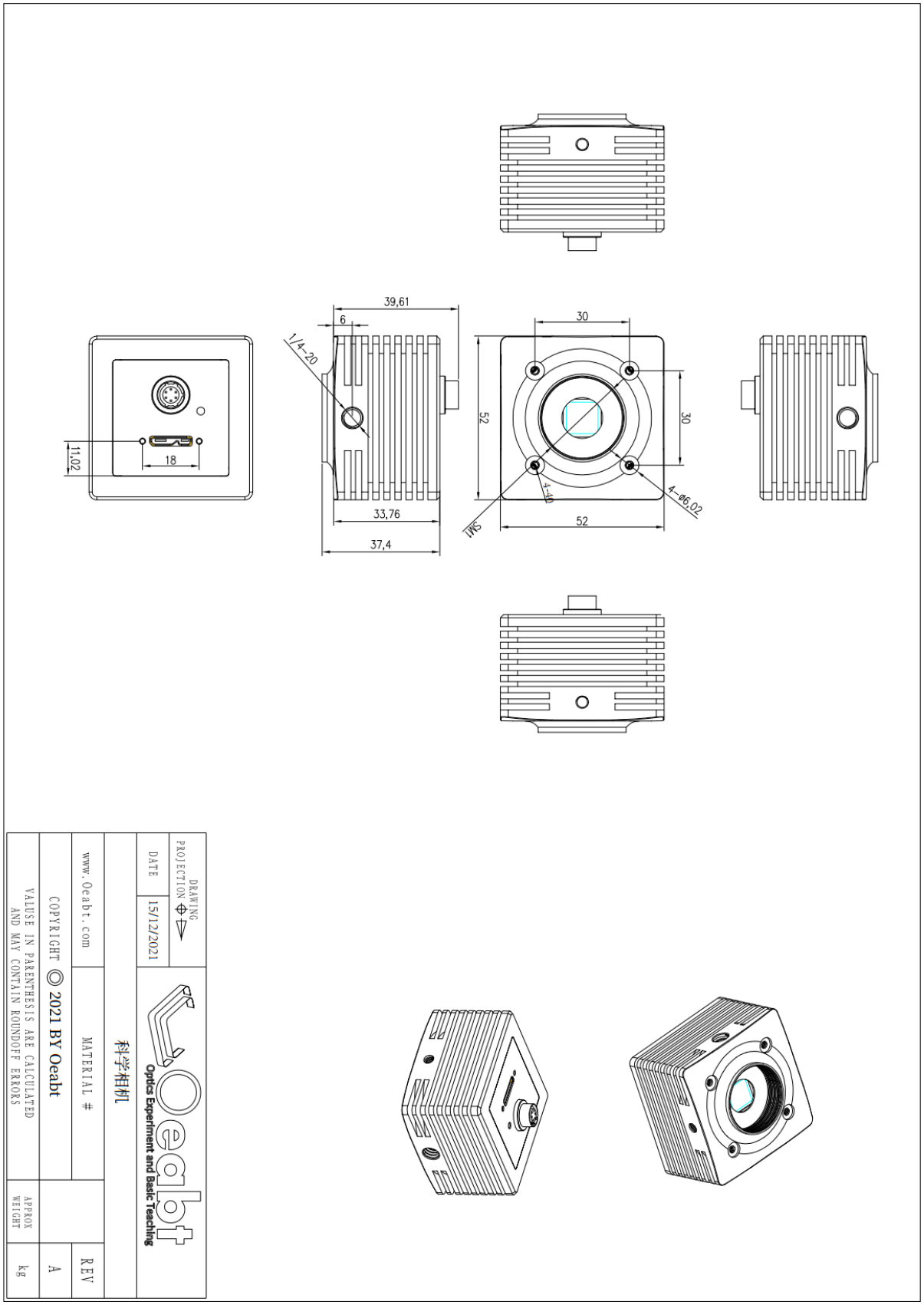

1.85μm
· 基础 The Basics
· 科研 The Research
· 精密 The Precision
科学相机
SCIENCE CAMERA
光学实验元器件
Oeabt
Digital I/O
USB 3.0
Oeabt 成像系统
微观世界·世界微观

- 130 万像素黑白科学相机；
- 全局曝光 130 万@60 帧/秒；
- FPGA+256Mb 硬件帧缓存，保证图像不丢帧，支持多台同步采集；
- 支持手动/自动曝光、LUT 查找表、GAMMA 查找表；
- USB3.0 接口， 5Gb/s 高速带宽，即插即用，无需外接供电；
- 支持 GPIO 光耦隔离外触发，信号滤波，闪光灯同步控制；
- 统一 API 软件开发包函数接口，支持 C、C++、C#、VB、LABVIEW、OPENCV、MIL、HALCON 等语言开发；
- 支持 Windows XP/7/10 32&64 位系统，Linux X86/ARM，Android 系统；
- CNC 加工高精度铝合金外壳，抗腐蚀，提供常规型和紧凑型外壳选项。

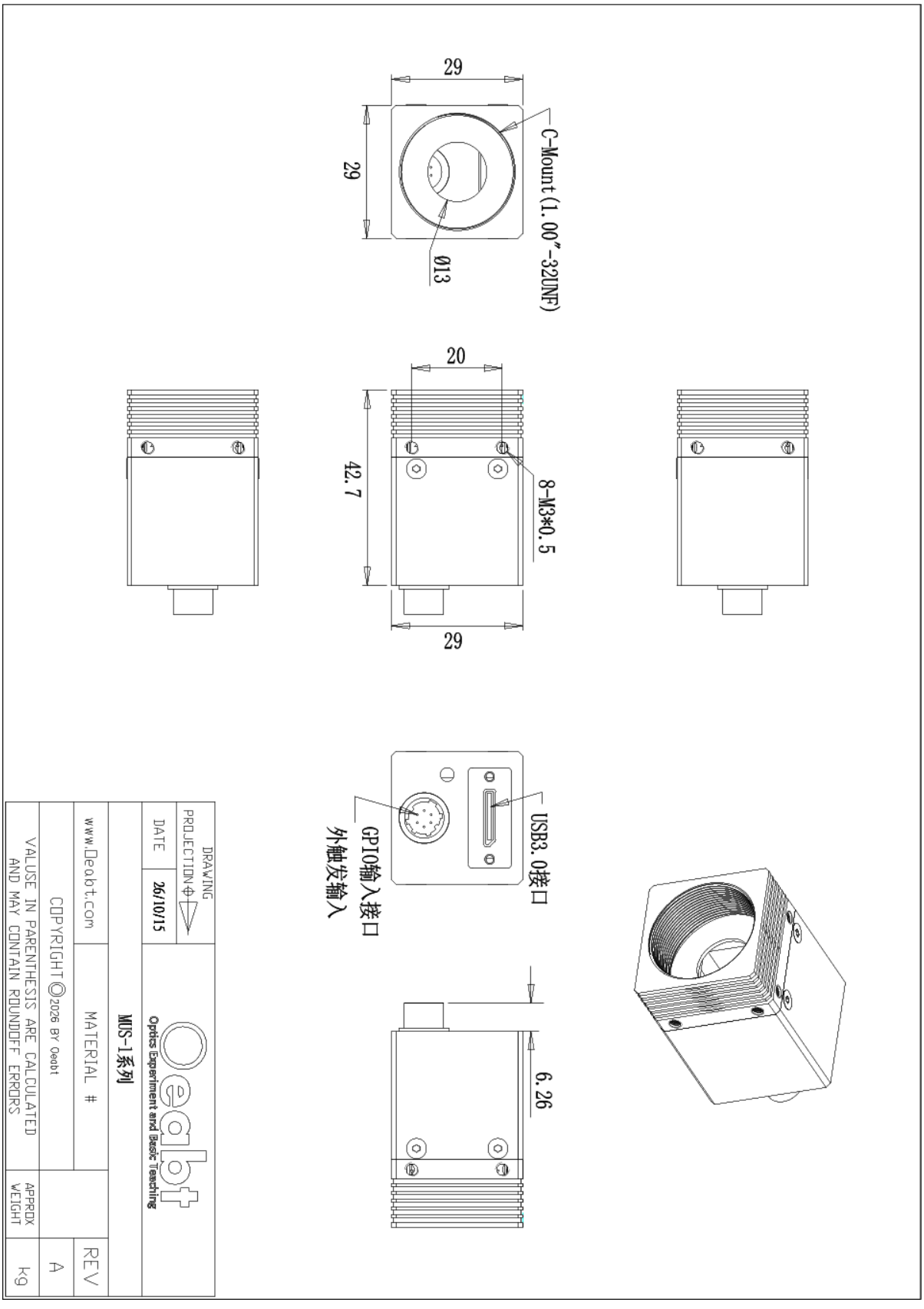
全局曝光相机型号参数表

产品型号	MUE130M-G-NIR / MUE130M-G-NIRI（紧凑型）
感光元件	近红外增强型 CMOS
色彩	黑白
读出模式	逐行
快门类型	全局曝光
有效像素	130 万
靶面尺寸	1/1.8″
像素尺寸	5.3μm
最大分辨率	1280x1024
帧速率	60fps
传输接口	USB3.0 接口、最大带宽 5.0Gbps
供电方式	USB3.0 接口供电、300～500mA@5V
图像存储	256Mb 帧存储器
输入输出	光耦隔离 GPIO、1 路外触发输入、1 路闪光灯输出、1 路 5V 输入/输出
基本功能	图像预览、图像采集、视频录像
可编程控制	预览视场 ROI、采集视场 ROI、SKIP/Binning 模式、对比度、亮度、Gamma 值、增益、曝光、噪点去除、锐化、聚焦评估、自定义序列号（0~255）、LUT 查找表
白平衡	自动/手动控制
曝光	自动/手动控制
图像格式	支持 RAW8,MONO8,BAYER24,BAYER32 图像预览采集，Jpeg、Bmp、Tiff 图像格式保存
标准支持	Twain、DirectSHOW
系统支持	Windows XP/7/10 32&64 位系统，Linux X86/ARM，Android 系统
SDK 开发包	支持 C、C#等开发语言，OPENCV、LABVIEW、HALCON、MIL 等第三方机器视觉软件
镜头接口	标配 C 接口
工作温度	-10℃至 60℃
储藏温度	-30℃至 70℃
整机尺寸	52mm X 52mm X 37.4mm / 紧凑型：29 X 29 X 42.7mm（宽 x 长 x 高）
相机重量	整机 *170g* / 紧凑型：*47.5g*（全铝合金外壳）
附件	3/5 米专用 USB3.0 固定线缆、6-pin HiroseGPIO 连接器、统一 API SDK 开发软件

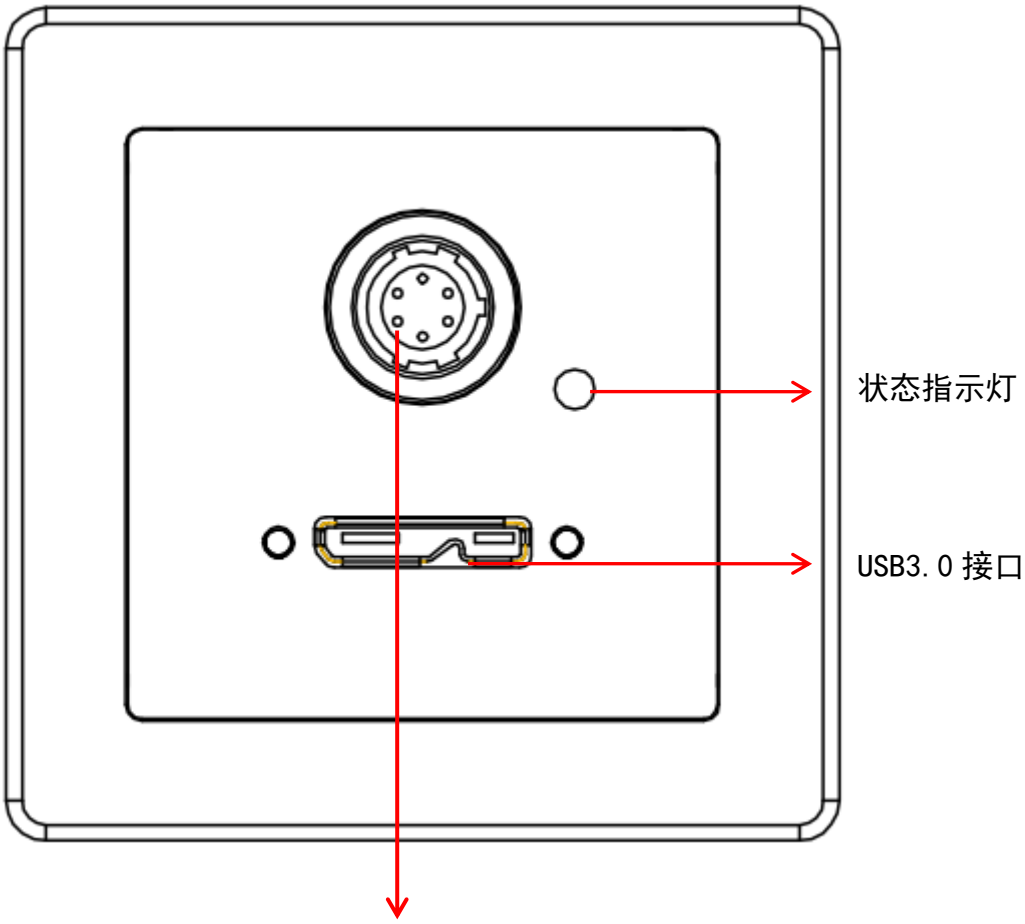
相机机械尺寸图

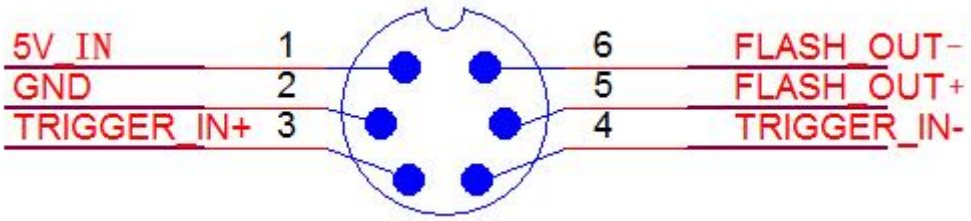

39,61
6
1/4-20
30
52
30
11,02
18
4-40
4-ø6,02
33,76
37,4
52
DRAWING
PROJECTION
DATE
15/12/2021
Oeabt
Optics Experiment and Basic Teaching
科学相机
www.Oeabt.com
MATERIAL #
REV
A
APPROX WEIGHT
kg
COPYRIGHT © 2021 BY Oeabt
VALUSE IN PARENTHESIS ARE CALCULATED AND MAY CONTAIN ROUNDOFF ERRORS

紧凑型相机机械尺寸图


29
29
C-Mount(1.00"-32UNF)
Ø13
20
42.7
8-M3*0.5
29
USB3.0接口
GPIO输入接口
外触发输入
6.26
DRAWING
PROJECTION
DATE
26/10/15
MUS-1系列
www.Oeabt.com
MATERIAL #
COPYRIGHT © 2026 BY Oeabt
VALUSE IN PARENTHESIS ARE CALCULATED AND MAY CONTAIN ROUNDOFF ERRORS
APPROX WEIGHT
kg
A
REV

接口说明





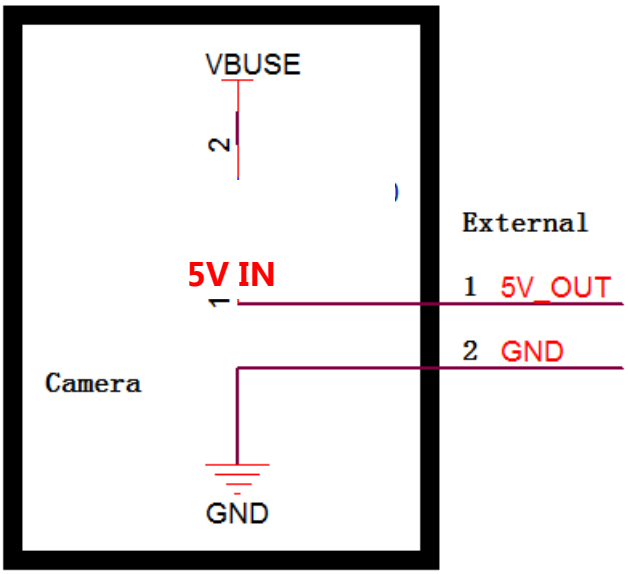
外触发头序号	1	2	3	4	5	6
线缆颜色	红	黑	黄	白	灰	棕
功能定义	5V IN	GND	TRIGGER_IN+	TRIGGER_IN-	FLASH_OUT+	FLASH_OUT-

状态指示灯

当相机上电后状态指示灯显示红灯表示配置 sensor 成功，状态指示灯闪烁表示采集图像传送数据正常。

电源接口

在计算机 USB 接口供电不足的情况下，可以给相机的提供外部供电，供电标准为 5V@500mA。



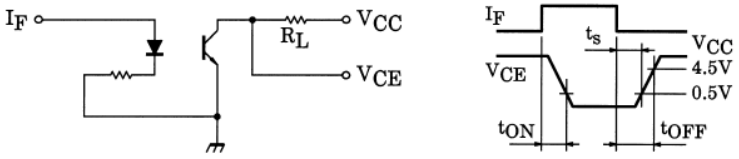
GPIO 输入接口（外触发输入）

下图为外触发输入的原理图,输入信号通过光耦 TLP281 进行隔离，TLP281 参数请参考附录 器件手册。

Switching Characteristics (Ta = 25℃)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Rise Time	t_r	V_{CC} = 10 V, I_C = 2 mA R_L = 100Ω	—	2	—	μs
Fall Time	t_f		—	3	—	
Turn-On Time	t_{on}		—	3	—	
Turn-Off Time	t_{off}		—	3	—	
Turn-On Time	t_{ON}	R_L = 1.9 kΩ (Fig.1) V_{CC} = 5 V, I_F = 16 mA	—	2	—	μs
Storage Time	t_s		—	25	—	
Turn-Off Time	t_{OFF}		—	40	—	

(Fig.1)SWITCHING TIME TEST CIRCUIT



TLP281 转换性能：

相机内部光耦 VCC=5V，若 IF=16mA，那么外触发输入**上升沿延时为 2μs，下降沿延时为 25μs**；

当使用 TRIGGER_IN+为触发源时,触发电平范围为 0V~+5V.如果触发源电平超出此范围,需外接限流电阻,使光耦工作在典型电流 10mA 以下。限流电阻的计算公式如下:

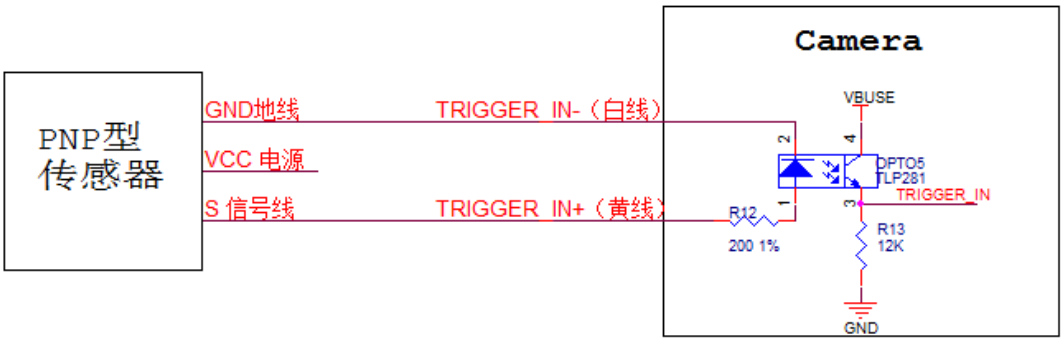
R = 100 x (Vin − 0.7) − R0

Vin 为触发源电平

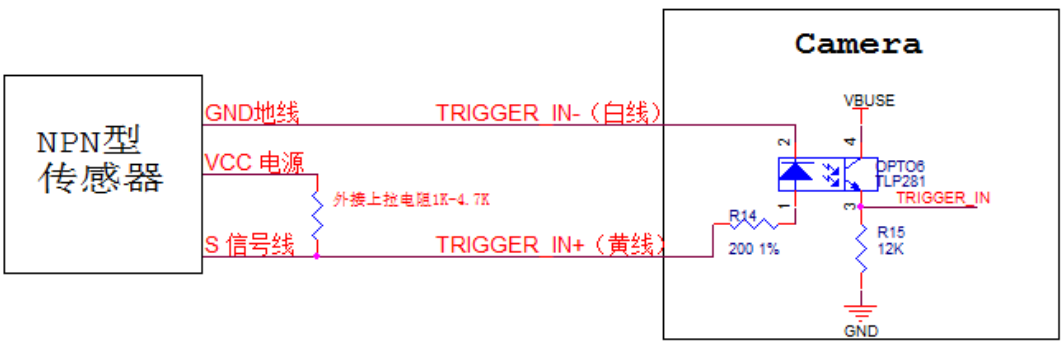
R0 为相机内部的串联电阻 200Ω

R 为外部需要串联的电阻

在正常温度条件下(0~+50℃),光耦的最大工作电流为 50mA,典型工作电流为 10mA,如果超过了最大允许电流，光耦有可能会被烧毁。下图为 PNP 型传感器和 NPN 型传感器与相机外触发连接示意图。

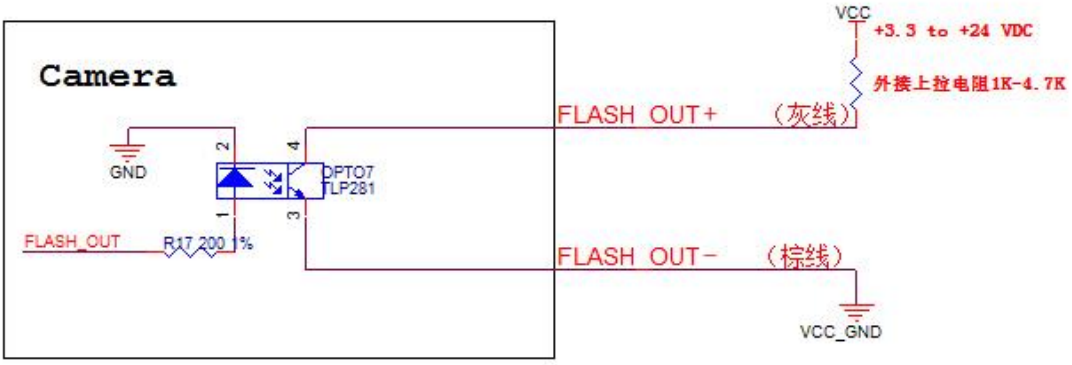


PNP型传感器连接示意图

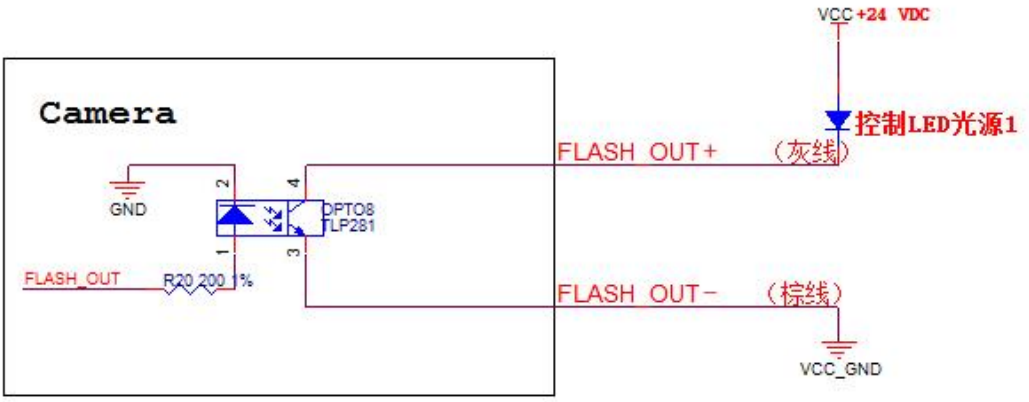


NPN型传感器连接示意图

GPIO 输出接口（闪光灯输出）

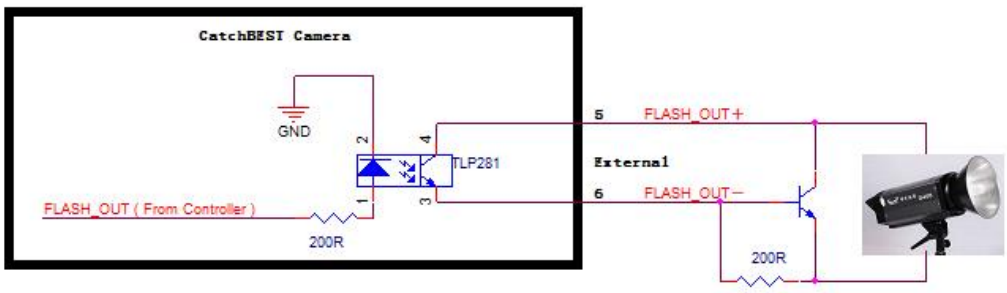


电平输出方式连接示意图

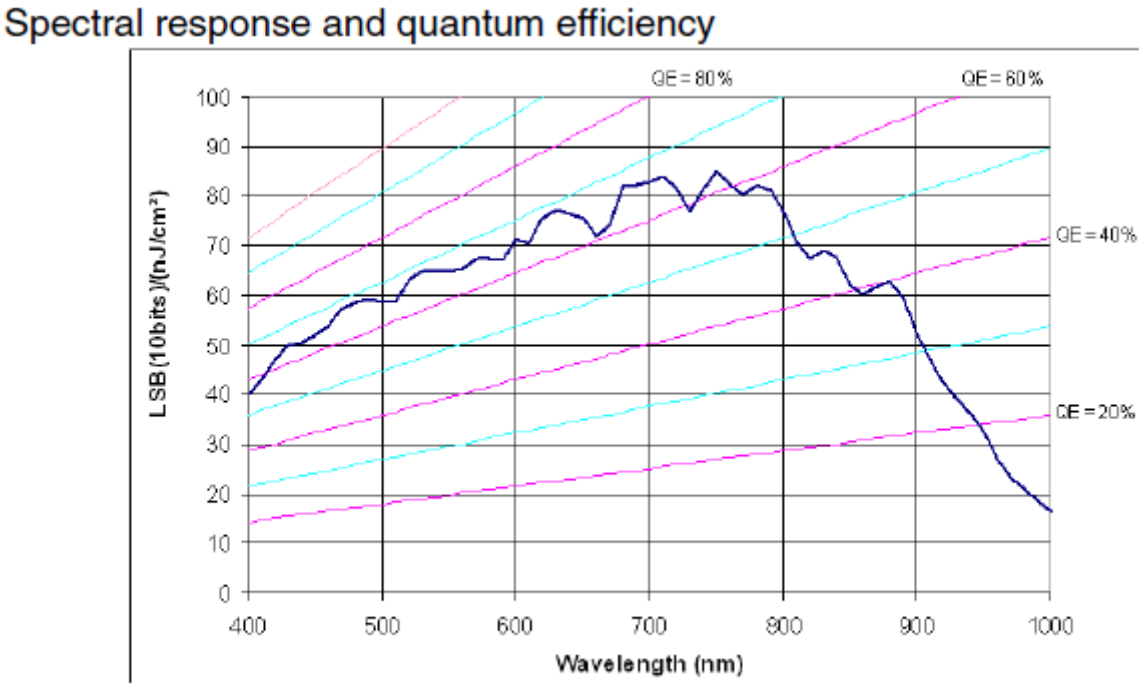


开关量输出方式连接示意图

对于一些有上拉输入的闪光灯（我们可以通过测量闪光灯同步输入的引脚来判断是否有上拉输入，如果我们测量到一个引脚有电平信号，则可以判断闪光灯内部有上拉的电平，比如小霸王 K-150A 型号闪光灯，同步触发引脚一端为+5V，另一端为 GND），可以使用下图的连接方法：



相机相应曲线图表



MUE130M-G-NIR

附录 1： 《TLP281 器件手册》

附录 2： 《SENSOR EV76C661 技术参数手册 》

附录 3： 《FPGA ALTERA CycloneIV 技术参数手册》

TOSHIBA PHOTOCOUPLER GaAs IRED & PHOTO-TRANSISTOR

TLP281,TLP281-4

PROGRAMMABLE CONTROLLERS

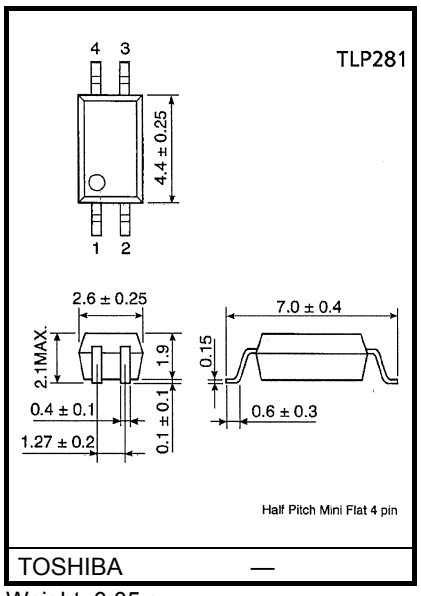
AC/DC-INPUT MODULE

PC CARD MODEM(PCMCIA)

TLP281 and TLP281-4 is a very small and thin coupler, suitable for surface mount assembly in applications such as PCMCIA Fax modem, programmable controllers.
TLP281 and TLP281-4 consist of photo transistor, optically coupled to a gallium arsenide infrared emitting diode.

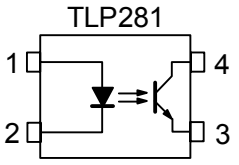
- Collector-Emitter Voltage : 80 V (MIN)
- Current Transfer Ratio : 50% (MIN)
  Rank GB : 100% (MIN)
- Isolation Voltage : 2500 Vrms (MIN)
- UL Recognized : UL1577 , File No. E67349
- BSI Approved : BS EN 60065: 2002,
  : BS EN 60950-1: 2002
  Certificate No. 8143, 8144

Unit in mm

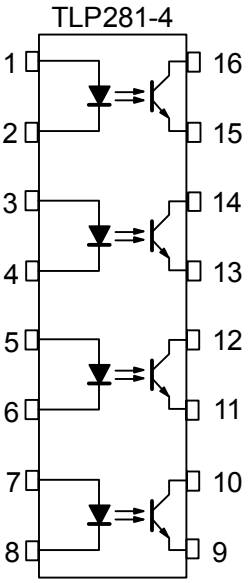


Weight: 0.05 g

Pin Configuration (top view)

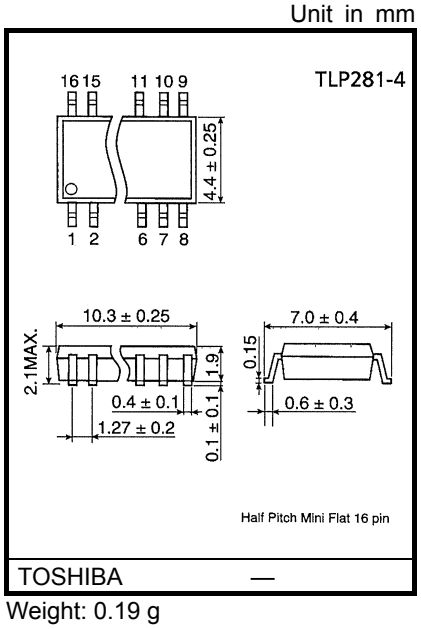


1:ANODE
2:CATHODE
3:EMITTER
4:COLLECTOR



1,3,5,7 :ANODE
2,4,6,8 :CATHODE
9,11,13,15 :EMITTER
10,12,14,16 :COLLECTOR

Unit in mm



Weight: 0.19 g

TYPE	Classi-Fication(*1)	Current Transfer Ration (%) (I_C / I_F) I_F = 5 mA, V_{CE} = 5 V, Ta = 25°C		Marking of Classification
		Min	Max	
TLP281	Blank	50	600	Blank ,Y■,YE,G,G■,GR,B,BL,GB
	Rank Y	50	150	YE
	Rank GR	100	300	GR
	Rank BL	200	600	BL
	Rank GB	100	600	GB
	Rank YH	75	150	Y■
	Rank GRL	100	200	G
	Rank GRH	150	300	G■
	Rank BLL	200	400	B
TLP281-4	Blank	50	600	Blank , GB
	Rank GB	100	600	GB

*1: Ex. rank GB: TLP281 (GB)

(Note): Application type name for certification test, please use standard product type name, i.e.
TLP281 (GB): TLP281−1 , TLP281−4 (GB): TLP281−4

Absolute Maximum Ratings (Ta = 25℃)

CHARACTERISTIC		SYMBOL	RATING		UNIT
			TLP281	TLP281−4	
LED	Forward Current	I_F	50		mA
	Forward Current Derating	ΔI_F /°C	−0.7 (Ta≥53°C)	−0.5 (Ta≥25°C)	mA /°C
	Pulse Forward Current	I_{FP}	1		A
	Reverse Voltage	V_R	5		V
	Junction Temperature	T_j	125		°C
DETECTOR	Collector-Emitter Voltage	V_{CEO}	80		V
	Emitter-Collector Voltage	V_{ECO}	7		V
	Collector Current	I_C	50		mA
	Collector Power Dissipation (1 Circuit)	P_C	150	100	mW
	Collector Power Dissipation Derating(Ta≥25°C) (1 Circuit)	ΔP_C /°C	−1.5	−1.0	mW /°C
	Junction Temperature	T_j	125		°C
Operating Temperature Range		T_{opr}	−55~100		°C
Storage Temperature Range		T_{stg}	−55~125		°C
Lead Soldering Temperature		T_{sol}	260 (10s)		°C
Total Package Power Dissipation (1 Circuit)		P_T	200	170	mW
Total Package Power Dissipation Derating (Ta≥25°C) (1 Circuit)		ΔP_T /°C	−2.0	−1.7	mW /°C
Isolation Voltage (Note1)		BV_S	2500(AC,1min,R.H.≤60%)		Vrms

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

(Note1) Device considered a two terminal device : LED side pins shorted together and DETECTOR side pins shorted together.

Individual Electrical Characteristics (Ta = 25℃)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
LED	Forward Voltage	V_F	I_F = 10 mA	1.0	1.15	1.3	V
	Reverse Current	I_R	V_R = 5 V	—	—	10	μA
	Capacitance	C_T	V = 0, f = 1 MHz	—	30	—	pF
DETECTOR	Collector-Emitter Breakdown Voltage	$V_{(BR)\ CEO}$	I_C = 0.5 mA	80	—	—	V
	Emitter-Collector Breakdown Voltage	$V_{(BR)\ ECO}$	I_E = 0.1 mA	7	—	—	V
	Collector Dark Current (Note2)	I_{CEO}	V_{CE} = 48 V, Ambient Light Below (100 ℓx)	—	0.01 (2)	0.1 (10)	μA
			V_{CE} = 48 V, Ta = 85°C Ambient Light Below (100 ℓx)	—	2 (4)	50 (50)	μA
	Capacitance (Collector to Emitter)	C_{CE}	V = 0, f = 1 MHz	—	10	—	pF

(Note 2) Because of the construction,leak current might be increased by ambient light.
Please use photocoupler with less ambient light.

Coupled Electrical Characteristics (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Current Transfer Ratio	I_C / I_F	I_F = 5 mA, V_{CE} = 5 V	50	—	600	%
		Rank GB	100	—	600	
Saturated CTR	I_C / $I_{F\ (sat)}$	IF = 1 mA, VCE = 0.4 V	—	60	—	%
		Rank GB	30	—	—	
Collector-Emitter Saturation Voltage	$V_{CE\ (sat)}$	I_C = 2.4 mA, I_F = 8 mA	—	—	0.4	V
		I_C = 0.2 mA, I_F = 1 mA	—	0.2	—	
		Rank GB	—	—	0.4	
Off-State Collector Current	$I_{C\ (off)}$	V_F = 0.7 V, V_{CE} = 48 V	—	—	10	μA

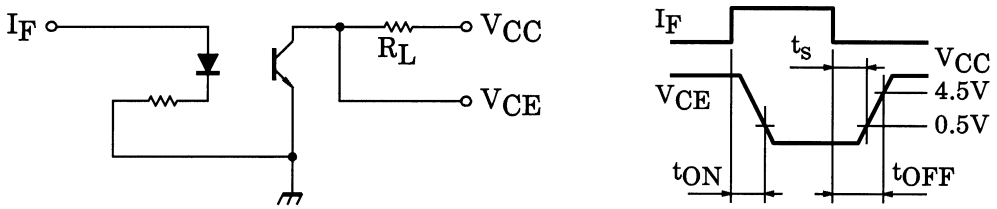
Isolation Characteristics (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Capacitance (Input to Output)	C_S	V_S = 0 V, f = 1 MHz	—	0.8	—	pF
Isolation Resistance	R_S	V_S = 500 V, R.H.≤60%	5×10^{10}	10^{14}	—	Ω
Isolation Voltage	BV_S	AC , 1 minute	2500	—	—	Vrms
		AC , 1 second,in OIL	—	5000	—	
		DC , 1 minute, in OIL	—	5000	—	Vdc

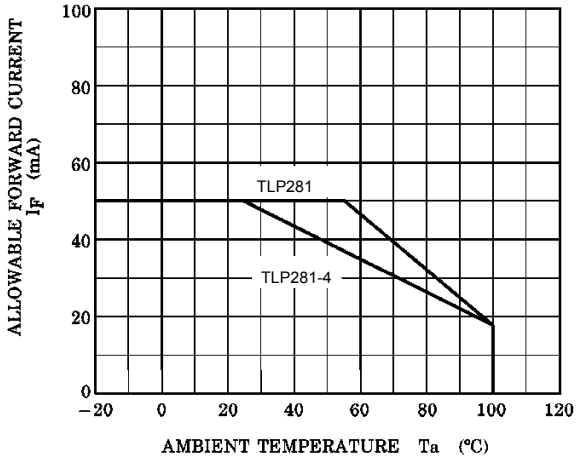
Switching Characteristics (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Rise Time	t_r	V_{CC} = 10 V, I_C = 2 mA R_L = 100Ω	—	2	—	μs
Fall Time	t_f		—	3	—	
Turn-On Time	t_{on}		—	3	—	
Turn-Off Time	t_{off}		—	3	—	
Turn-On Time	t_{ON}	R_L = 1.9 kΩ (Fig.1) V_{CC} = 5 V, I_F = 16 mA	—	2	—	μs
Storage Time	t_s		—	25	—	
Turn-Off Time	t_{OFF}		—	40	—	

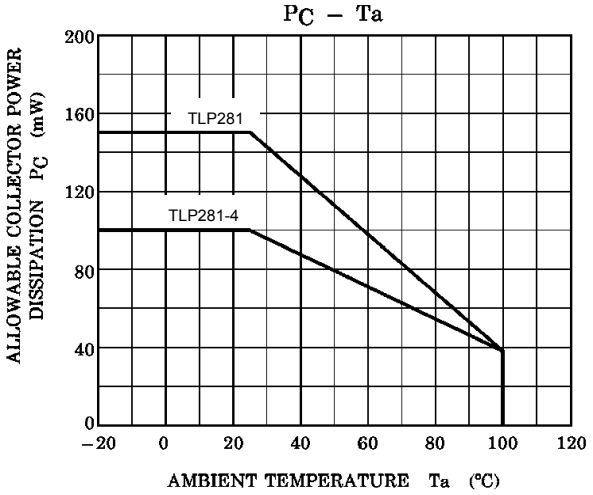
(Fig.1)SWITCHING TIME TEST CIRCUIT



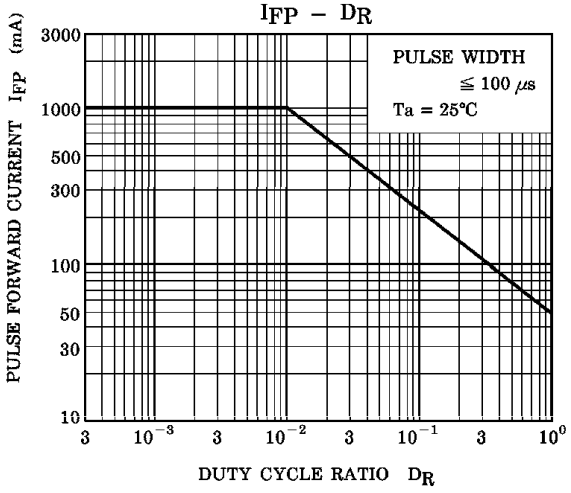
I_F – Ta



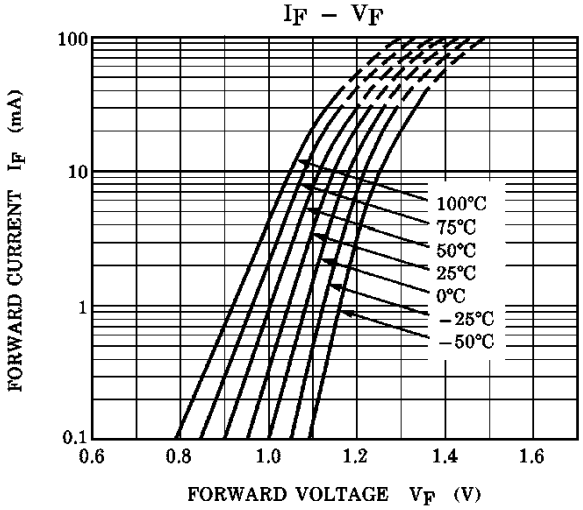
P_C – Ta



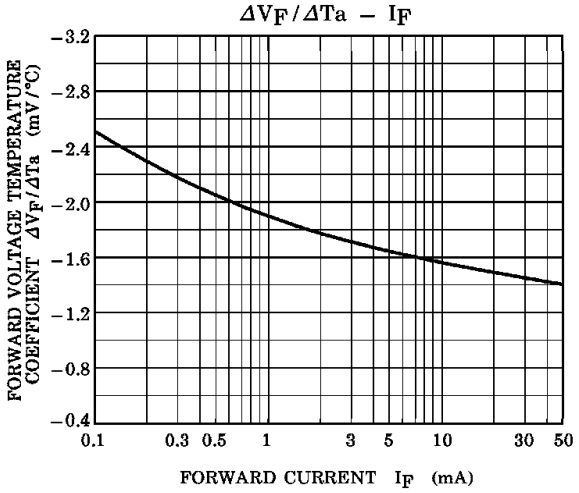
I_{FP} – D_R



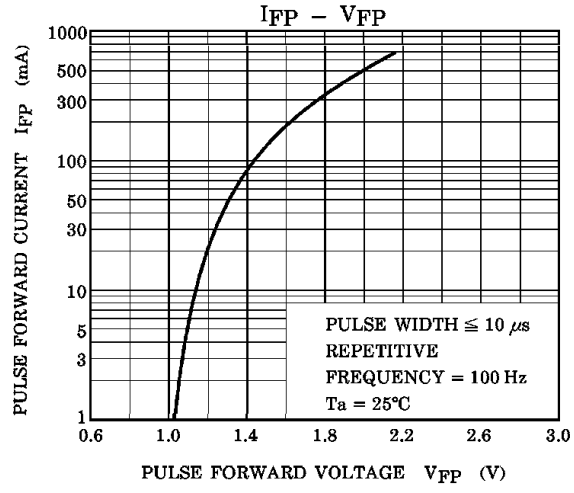
I_F – V_F



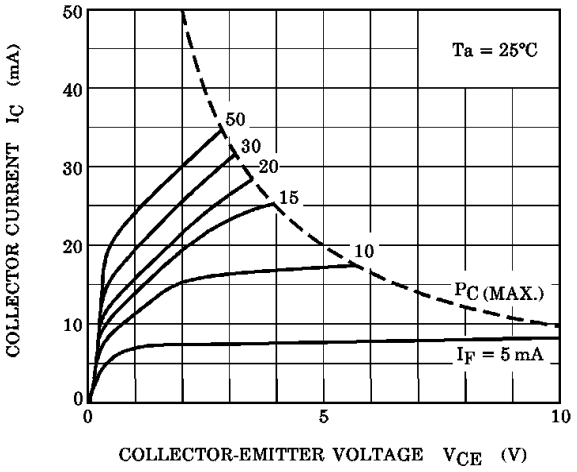
$\Delta V_F / \Delta Ta$ – I_F



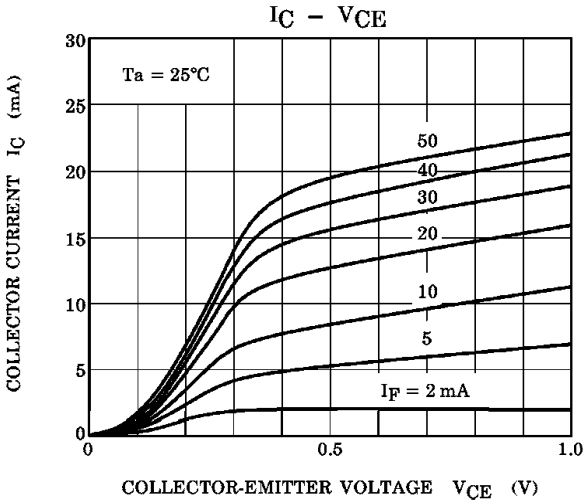
I_{FP} – V_{FP}



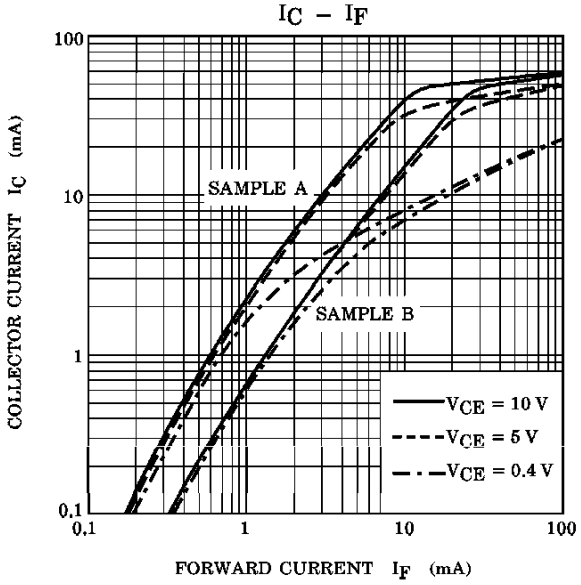
$I_C - V_{CE}$



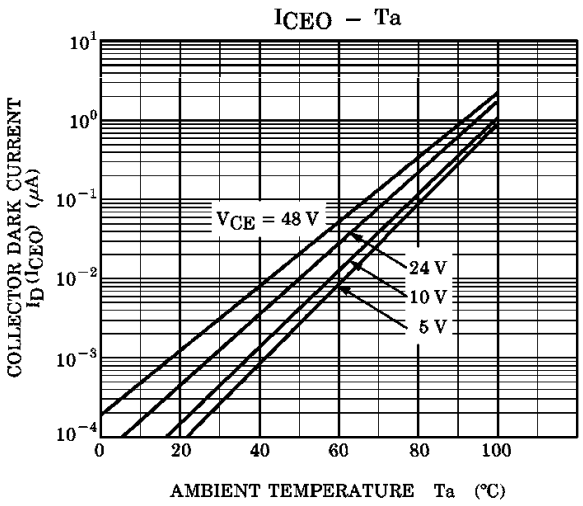
$I_C - V_{CE}$



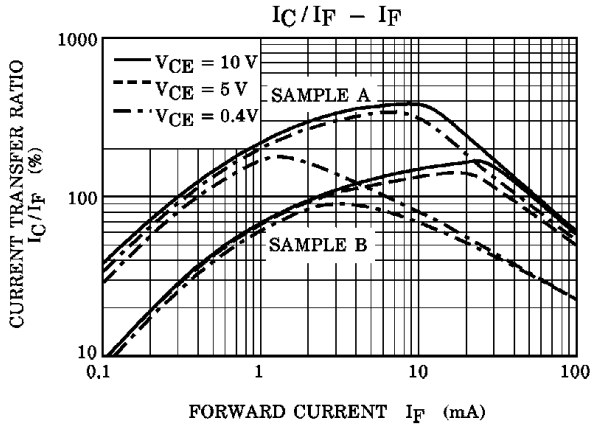
$I_C - I_F$



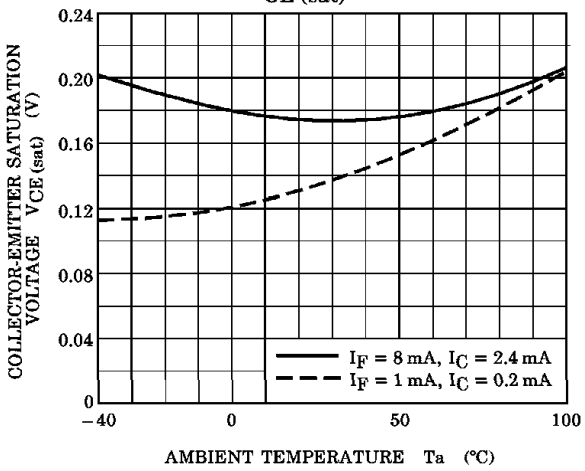
$I_{CEO} - Ta$



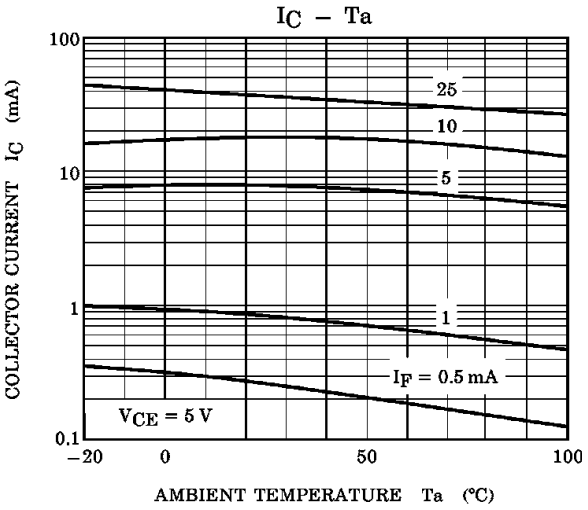
$I_C / I_F - I_F$



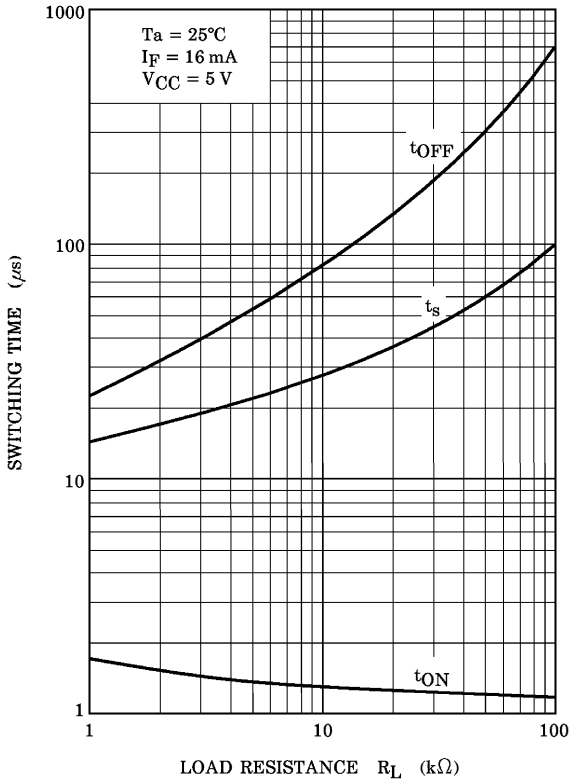
V_{CE} (sat) – Ta



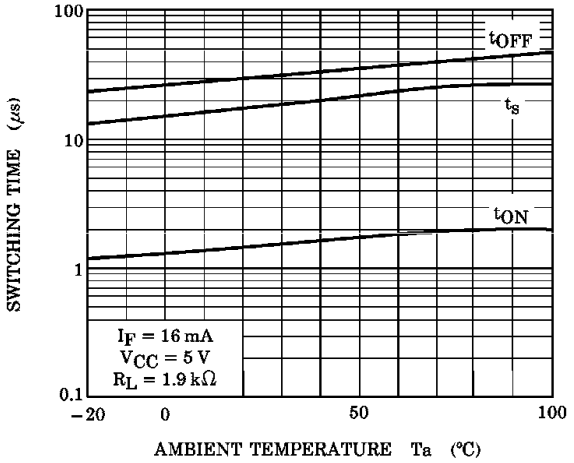
I_C – Ta



SWITCHING TIME – R_L



SWITCHING TIME – Ta



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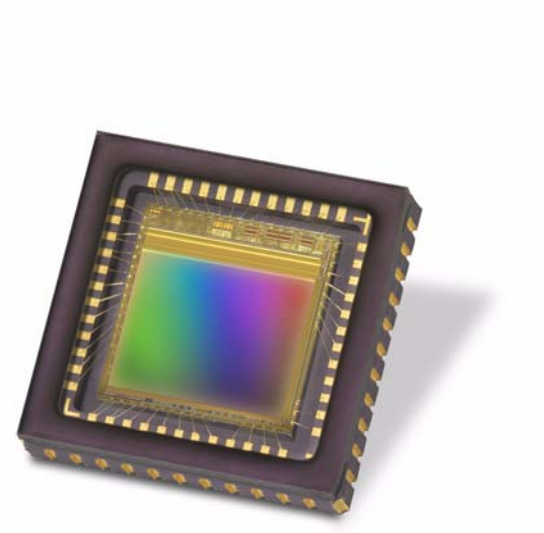
EV76C661
1.3 Mpixels B&W and Color CMOS Image Sensor

附录2：《SENSOR EV76C661技术参数手册》

Datasheet

Features

- 1.3 million (1280 x 1024) pixels, 5.3 µm square pixels with micro-lens
- Optical format 1/1.8"
- 60 fps@ full resolution
- Embedded functions:
  - Image Histograms and Context output
  - Sub-sampling / binning
  - Multi-ROI (including 1 line mode)
  - Defective pixel correction
  - PLL with 5 to 50 MHz input frequency range (compatible with dithered master clock)
  - High dynamic range capabilities
  - Time to Read improvement (Abort image and Good first image)
- Timing modes:
  - Global shutter in serial and overlap modes
  - Rolling shutter allowing lowest readout noise and global reset
- Output format 8 or 10 bits parallel plus synchronization
- SPI controls
- Control input pins: Trigger, Reset
- Light control output
- 3.3 V and 1.8 V power supplies



Performance Characteristics

- Low power consumption (200 mW)
- High sensitivity at low light level
- Operating temperature [-30° to +65°C]
- Peak QE > 65%

Available Sensor Types

- B&W
- Color (Bayer arrangement)
- Other (custom CFA) by request

Applications

- Surveillance IP/CCTV cameras
- Biometrics/Medical Imaging
- Automotive Vision
- Industrial Machine Vision, Barcode Reading and Scanning

Introduction

The EV76C661 is a 1.3 million pixel CMOS image sensor and a member of “Ruby” family. It is suitable for many different types of application where superior performance is required. The innovative pixel design offers excellent performance in low-light conditions with an electronic global (true snapshot) shutter, and offers a high readout speed at 60 fps in full resolution. Its very low power consumption makes it well suited for battery powered applications.

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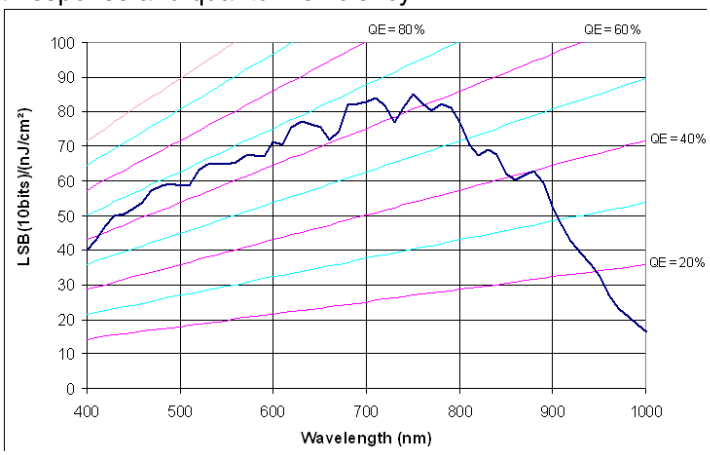
1. Typical Performance Data

Table 1-1. Typical electro-optical performance @ 25°C and 65°C, nominal pixel clock

Parameter		Unit	Typical value	
Sensor characteristics	Resolution	pixels	1280 (H) × 1024 (V)	
	Image size	mm inches	6.9 (H) × 5.5 (V) - 8.7 (diagonal) ≈ 1/1.8	
	Pixel size (square)	µm	5.3 × 5.3	
	Aspect ratio		5 / 4	
	Max frame rate	fps	60 @ full format	
	Pixel rate	Mpixels / s	90 -> 120	
	Bit depth	bits	10	
Pixel performance			**@25°C**	**@65°C**
	Dynamic range (1)	dB	>63	>60
	Qsat	ke-	8.4	
	SNR Max	dB	39	39
	MTF at Nyquist, λ=550 nm	%	50	
	Dark signal (2)	LSB_{10}/s	38	830
	DSNU(2)	LSB_{10}/s	21	220
	PRNU (3) (RMS)	%	<1.5	
	Responsivity (4)	LSB_{10}/(Lux.s)	13000	
Electrical interface	Power supplies	V	3.3 & 1.8	
	Power consumption: Functional (5) Standby	mW µW	< 200 mW 180	

1. In electronic rolling shutter (ERS) mode.
2. Min gain, 10 bits.
3. Measured @ Vsat/2, min gain.
4. 3200K, window with AR coating, IR cutoff filter BG38 2 mm.
5. @ 60 fps, full format, with 10 pF on each output.

Figure 1-1. Spectral response and quantum efficiency



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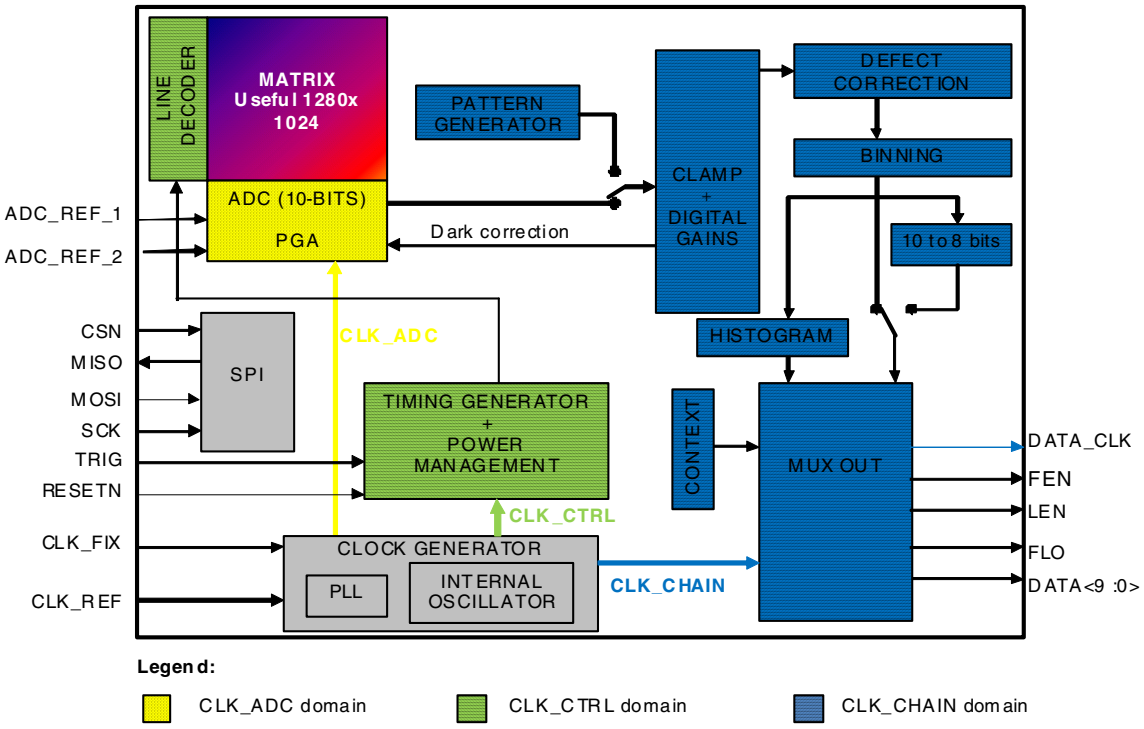
2. Sensor Overview

Figure 2-1. Block diagram



Detailed descriptions of the I/O signals and blocks are given in the datasheet sections listed in Table 2-1
See Section 21. for the device pinout information.

Table 2-1. Quick reference table for block diagram

Signal name	I/O	Description	Reference
ADC_REF1&2	I	ADC reference voltages	Section 5.2
CSN	I	SPI chip select	Section 17.
MISO	O	SPI data output	
MOSI	I	SPI data input	
SCK	I	SPI clock	
TRIG	I	Trigger input	Section 18.
CLK_REF	I	Reference clock input	Section 14.
CLK_FIX	I	Fixed clock input	
RESETN	I	Sensor reset	Section 18.
DATA<9:0>	O	10-bit data output bus	Section 19.
FEN	O	Vertical sync output	
LEN	O	Horizontal sync output	
FLO	O	Illumination control output	Section 19.6
DATA_CLK	O	Output clock	

List of blocks	Reference
Matrix	Section 4.
ADC + PGA	Section 5.
Clamp + digital gain	Section 6. & 7.
Defect correction	Section 8.
Binning	Section 9.
Histogram	Section 10.
10->8 bits	Section 11.
Context	Section 12.
Mux out	Section 13.
Timing and power management	Section 14.
Clock generator	Section 15.
Pattern generator	Section 16.
SPI	Section 17.

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3. Standard Configuration

3.1 Sensor Settings

The static configuration required to allow image capture is as follows:

- All ground pins connected.
- All power supply pins with the same name connected together.
- SPI pins connected to the host controller.
- 1.8 V pins and 3.3 V pins powered-on.
- Input clock driving the CLK_REF input pin.
- RESETN pin held at high level after the power-on sequence. See Section 18.1.1
- STANDBY state is deactivated by writing 0 in the ***stdby_rqst*** bit in the **<reg_ctrl_cfg>** register. See Section 17.3.8
- Image capture is triggered by a high level on the TRIG pin or setting the ***trig_rqst*** bit in the **<reg_ctrl_cfg>** register. See Section 17.3.8

For improved performance, VDD33A and VDD18A must be noise-free. The best way to decouple VDD33A and to increase the power supply rejection ratio is to use a linear regulator dedicated to the image sensor. To prevent noise on VDD18A an inductor can be used.

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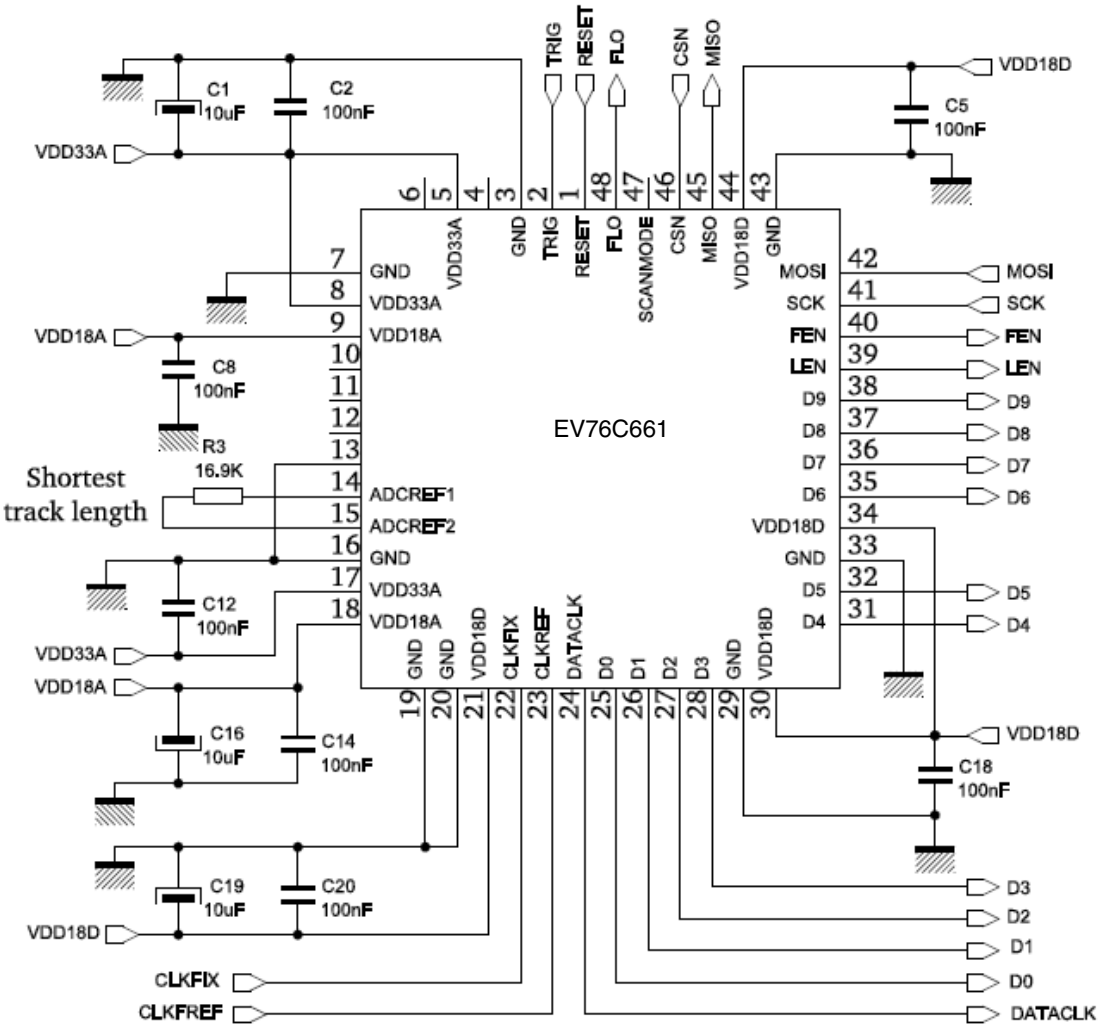
3.2 Application Information

Figure 3-1. Required external components



It is recommended to use X7R for all the 100 nF capacitors.

Reset pin has an internal pull-up.

Pins 4, 6, 10, 11 and 12 should not be electrically connected (floating).

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3.3 Electrical Levels

Table 3-1. DC Characteristics @ 25°C

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Analog power supply relative to GND	VDD33A	3.15	3.3	3.45	V
Digital power supply relative to GND	VDD18D	1.6	1.8	2	V
Analog power supply relative to GND	VDD18A	1.6	1.8	2	V
Power supply consumption (1)	P		190		mW
Supply current at 60 fps (VDD33A pin)	I_{VDD33A}		20		mA
Supply current at 60 fps (VDD18A pin)	I_{VDD18A}		25		mA
Supply current at 60 fps (VDD18D pin)	I_{VDD18D}		30		mA
Standby supply current on VDD33A pin	$I_{VDD33A(STBY)}$		0		
Standby supply current on VDD18A pin	$I_{VDD18A(STBY)}$		0		
Standby supply current on VDD18D pin (2)	$I_{VDD18D(STBY)}$		50	100	µA
IDLE supply current on VDD33A pin	$I_{VDD33A(IDLE)}$		6		mA
IDLE supply current on VDD18A pin	$I_{VDD18A(IDLE)}$		0		mA
IDLE supply current on VDD18D pin	$I_{VDD18D(IDLE)}$		7		mA
CMOS in/out					
Input voltage low level	V_{IL}			0.3 V_{DD18}	V
Input voltage high level	V_{IH}	0.7 V_{DD18}			V
Input pin capacitance (3)	C_{IN}		4		pF
Output voltage low level	V_{OL1}			0.55	V
Output voltage high level	V_{OH1}	V_{DD18}-0.55			V
Output current @ VOH (4)	I_{OH}	-10			mA
Output current @ VOL (4)	I_{OL}			10	mA
Input leakage current (5)	I_L	-1		1	µA
ADC_REF current (6)	I_{ADC_REF}		100		µA

1. Digital output loads =10 pF
2. $I_{VDD18D(STDBY)}$ with SPI on, without communication and without CLK_REF input.
3. CLCC48 package
4. On all output pins
5. On all digital input pins
6. On ADC_REF pins

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4. Matrix

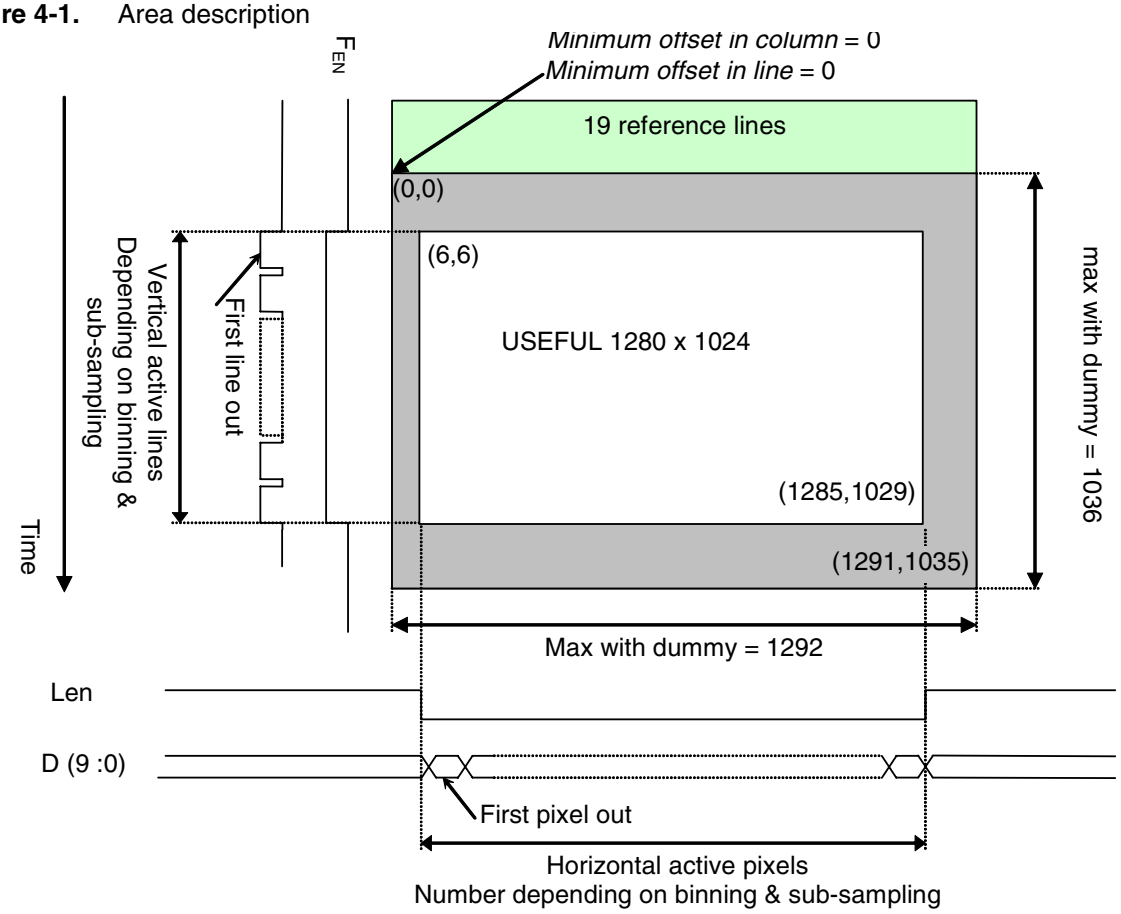
4.1 Useful Area Definition

The useful area is 1280 × 1024 pixels as shown in Figure 4-1.

19 optically shielded reference lines to allow the black level adjustment.

6 dummy illuminated pixels surround the useful area.

Figure 4-1. Area description



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4.2 CFA (Color Filter Array)

The following CFA types are implemented:

- Monochrome
- RGB Bayer filter

Other types are available on request.

As CFA choice does not require a silicon hardware change but only post-process, to allow correct configuration of binning, subsampling and color gains, the sensor must be configured by setting 1 in the *color_en* registerwhen a color sensor is used. Note that image size depends on this factor. See Section 4.5.3.1.

Table 4-1. Color of first pixel using the flip functions (depends on H&V offset parities)

		RoiX_0l_1 / RoiX_0c_1			
Flip H	Flip V	Odd/Odd	Odd/Even	Even/odd	Even/Even
N	N	Red	Green Red	Green Blue	Blue
N	O	Green Blue	Blue	Red	Green Red
O	N	Green Red	Red	Blue	Green Blue
O	O	Blue	Green Blue	Green Red	Red

RoiX_0l stands for ROI1_0l_1, Roi2_0l_1, Roi3_0l_1 & Roi4_0l_1. See Section 17.3.11, 17.3.12, 17.3.13, and 17.3.14 respect

RoiX_0c stands for Roi1_0c_1, Roi2_0c_1, Roi3_0c_1 & Roi4_0c_1. Section 17.3.11, 17.3.12, 17.3.13, and 17.3.14 respectively

It is recommended to keep:

- Roi_W_1 + Roi_0c_2 even
- Roi_h_1 + Roi_0l_2 even

Flip H & Flip V are under roi_flip_h & roi_flip_v control. See <reg_miscel2> in Section 17.3.4

4.3 Pixels

The matrix is composed of five transistor (5T) pixels. This structure supports either global shutter (GS) mode or electronic rolling shutter (ERS) mode (Section 18.2).

4.4 Lens CRA (Chief Ray Angle) compensation.

In order to better focus the light rays on the photodiode, the EV76C661 micro lenses are radially shifted to match the exit angles due to the external application lens. This results in improved efficiency and reduced corner shading.

This shift is linearly applied from center (0 shift) to corner (α angle).

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α is the corner CRA (Chief Ray Angle) defined as a mean value of the telecentricity of optics lenses that would be used with the sensor.

The sensor, optimized for a corner CRA of 12°, can be used with a range of telecentricity from 5° to 20° (estimated for fnumber f#/1.2).

Figure 4-2. Microlens Shifting

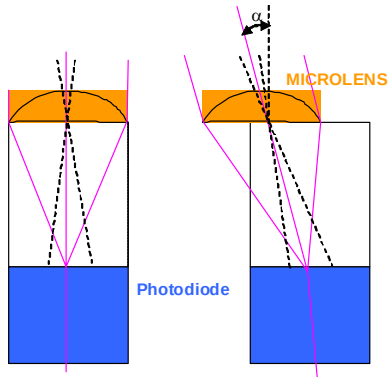
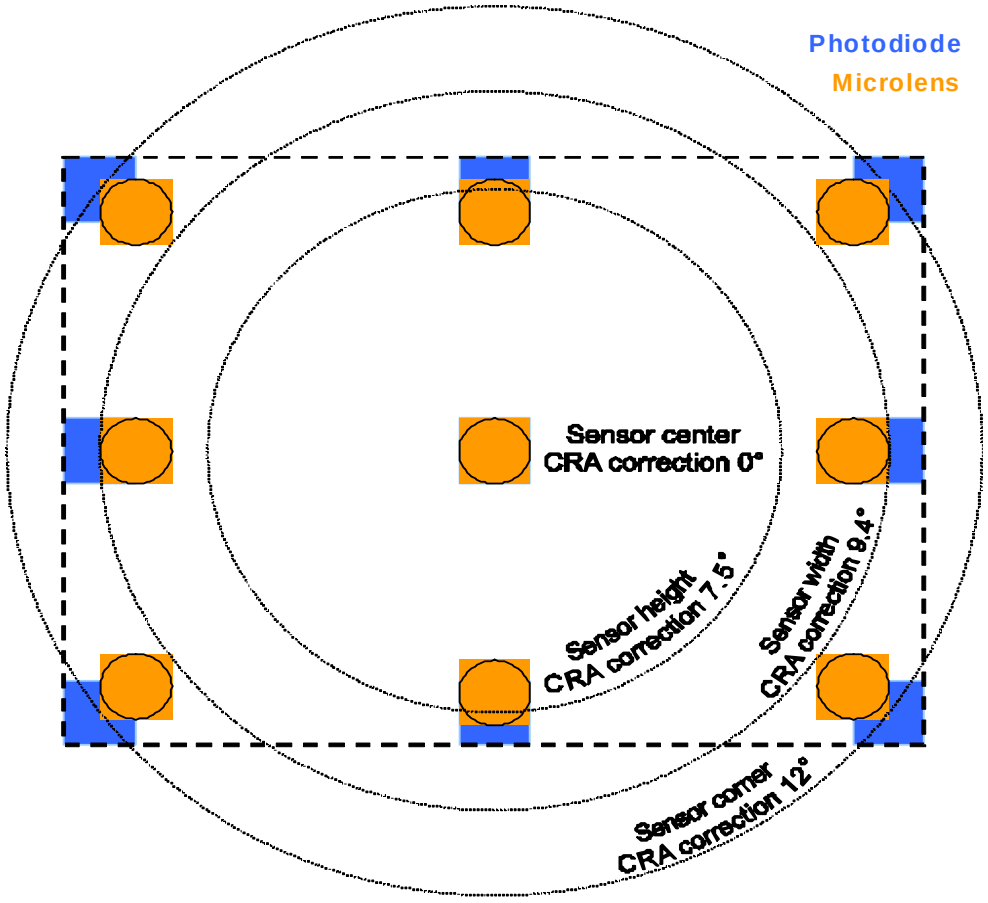


Figure 4-3. Lens CRA overview



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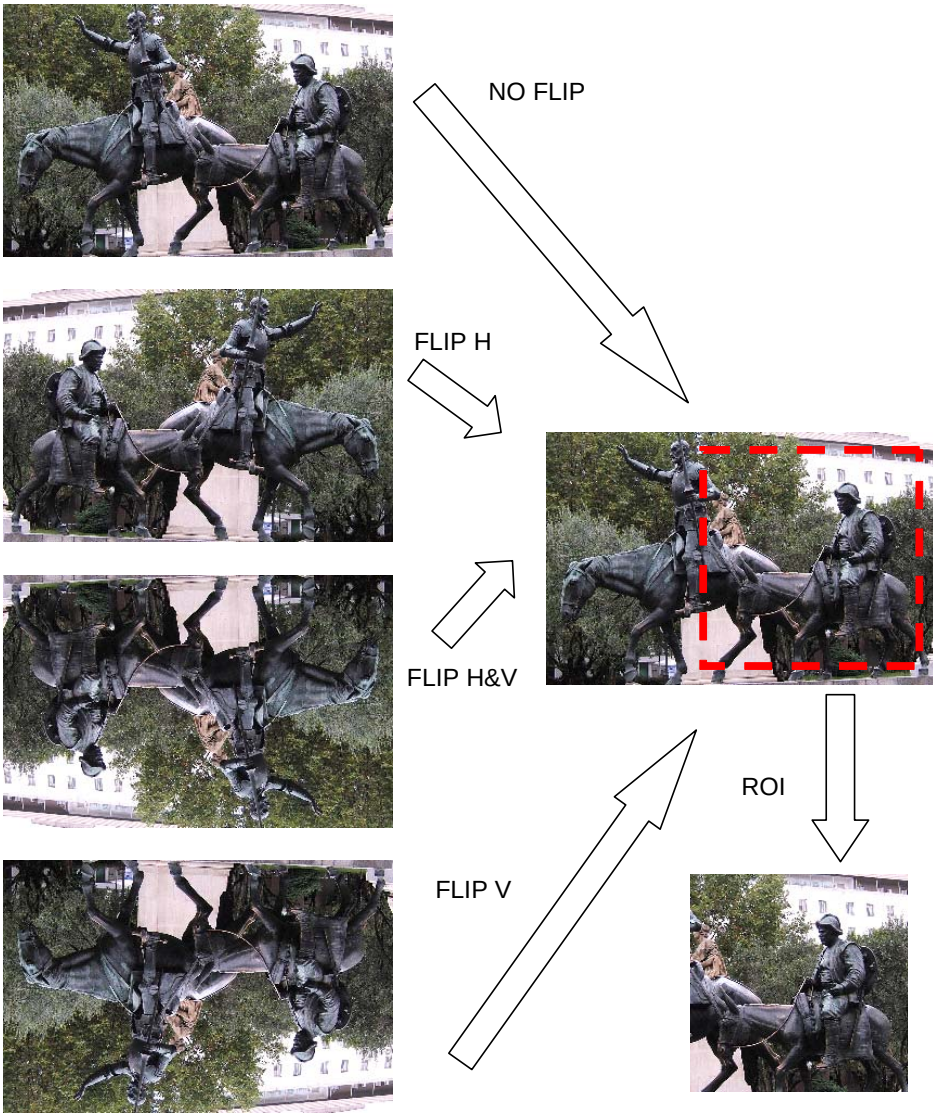
4.5 Region Of Interest (ROI)

4.5.1 Flip Functions

Flip functions are available to allow the application to use any type of lens (with or without mirror). The flip functions are controlled by programming the ***roi_flip_h*** and ***roi_flip_v*** bitfields in the **<reg_miscel2>** register. See Section 17.3.4. The ROI is applied on the flipped image.

The shielded lines for dark reference are always read first (except in expanded ROI mode selected by the ***roi_expanded*** bit in the **<reg_miscel2>** register (see Section 17.3.4) when whole lines may be read.

Figure 4-4. Flip effects



4.5.2 ROI Definition

All ROIs are defined in relation to the matrix and useful pixel area (as shown in Figure 4-1). The ROIs are defined before sub-sampling, defect correction and binning.

If a flip effect is used, ROI selection is done after the flip.

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4.5.3 Sub-Sampling and Windowing

- The sub-sampling function causes the sensor to read only 8 pixels over the selected factor. For example, a sub-sampling factor of 8 over 16 means that the sub-sampling ratio is 1:2. For color sensors, the algorithm is more complicated due to the Bayer organization.
  Sub-sampling is programmable with a ratio 1 to 32 in steps of 0.125. Different sub-sampling factors can be defined for horizontal and vertical directions. They are programmable using SPI commands: ***roiX_subs_v*** and ***roiX_subs_h*** in **<reg_roiX*>** (where X* is the number of the ROI 1, 2, 3 or 4 registers group) see Section 17.3.11, 17.3.12, 17.3.13, and 17.3.14 respectively.
- Windowing defines the size and position of the ROI. Windowing is defined in two dimensions: horizontal and vertical. The minimum width of the window is 16 columns and the minimum height is 1 line. The user has to define the height, width and offsets of the ROI through the SPI control bus for each ROI used. (See Section 4.5.4).

Windowing, sub-sampling and then binning are possible on the same image.

Figure 4-5. Combination of windowing, sub-sampling and binning example for a B&W image.

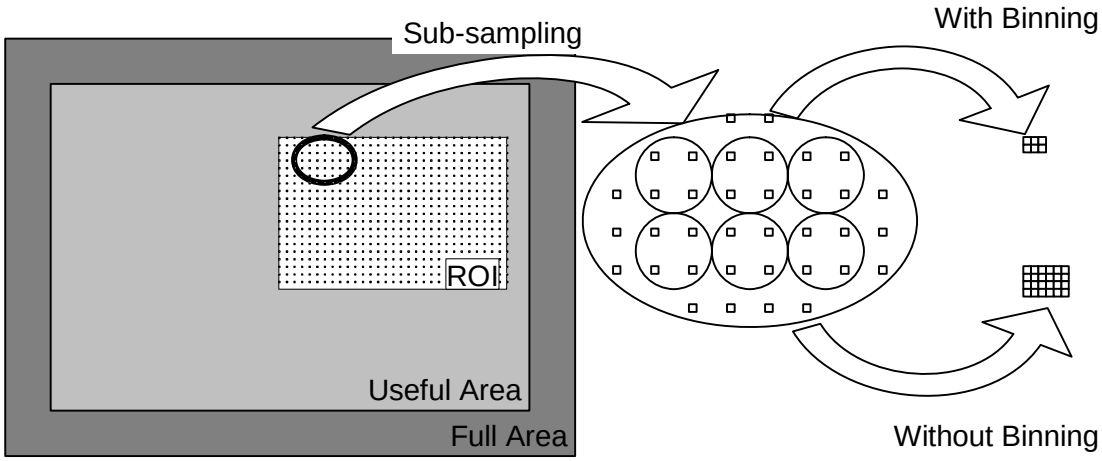
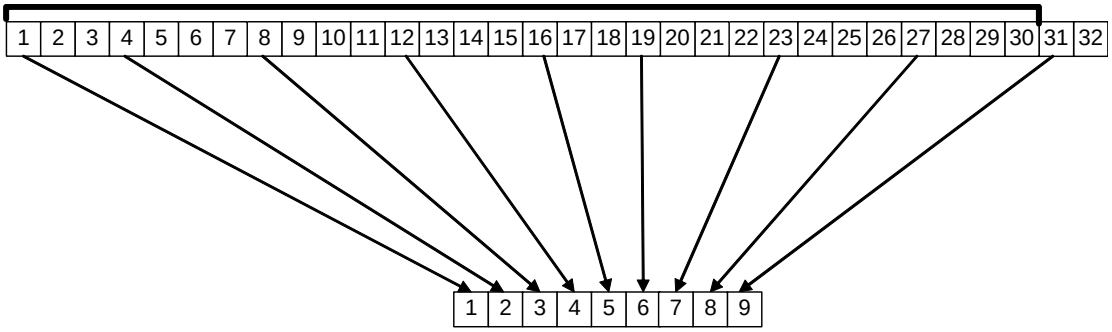


Figure 4-6. Sub-sampling example



With an 8/30 sub-sampling factor only these pixels (or lines) will be read:

- On the first group of 30 pixels: 1, 4, 8, 12, 16, 19, 23, 27
- On the second group of 30 pixels: 31, 34, 38…
- On the third group of 30 pixels: 61…

Roughly, the sub-sampled image format will be multiplied by 8/30=1/3.75. For more precise calculation of the output image size the following formulas must be used.

4.5.3.1 *Calculating the Image Output Size*

Image output sizes are determined by the following equations depending on:

- B&W or color version (***color_en*** in **<reg_miscel2>** see Section 17.3.4,
- Sub-sampling factor (***roiN_subs_v*** and ***roiN_subs_h*** in **<reg_roiN*>** see Section 17.3.11, 17.3.12, 17.3.13, and 17.3.14 respectively),
- Defect correction activation (***roi_ddc_en*** in **<reg_chain_cfg>** see Section 17.3.7),
- Binning activation (***roiN_binning_en*** in **<reg_chain_cfg>** see Section 17.3.7.

If *roiN_binning_en* = 0 AND *color_en* = 0

For ROI 1:

$$ROI_width = \mathrm{INT}\left(\frac{8 \times roi1_w_1}{roi1_subs_factor + 8}\right) + \mathrm{INT}\left(\frac{8 \times roi1_w_2}{roi1_subs_factor + 8}\right)$$

For ROI 2, 3 and 4:

$$ROI_width = \mathrm{INT}\left(\frac{8 \times roiN_w}{roiN_subs_factor + 8}\right)$$

If (*roiN_binning_en* = 1 AND *color_en* = 0) OR (*roiN_binning_en* = 0 AND *color_en* = 1)

For ROI 1:

$$ROI_width = 2 \times \left[\mathrm{INT}\left(\frac{4 \times roi1_w_1}{roi1_subs_factor + 8}\right) + \mathrm{INT}\left(\frac{4 \times roi1_w_2}{roi1_subs_factor + 8}\right)\right]$$

For ROI 2, 3 and 4:

$$ROI_width = 2 \times \mathrm{INT}\left(\frac{4 \times roiN_w}{roiN_subs_factor + 8}\right)$$

If *roiN_binning_en* = 1 AND *color_en* = 1

For ROI 1:

$$ROI_width = 4 \times \left[\mathrm{INT}\left(\frac{2 \times roi1_w_1}{roi1_subs_factor + 8}\right) + \mathrm{INT}\left(\frac{2 \times roi1_w_2}{roi1_subs_factor + 8}\right)\right]$$

For ROI 2, 3 and 4:

$$ROI_width = 4 \times \mathrm{INT}\left(\frac{2 \times roiN_w}{roiN_subs_factor + 8}\right)$$

Then, *width_out* is:

$$\rightarrow \quad width_out = \frac{ROI_width - 4 \times ddc_en}{2^{roiN_binning_en}}$$

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If *roiN_binning_en* = 0 AND *color_en* = 0

For ROI 1

$$ROI_height = \mathrm{INT}\left(\frac{8 \times roi1_h_1}{roi1_subs_factor + 8}\right) + \mathrm{INT}\left(\frac{8 \times roi1_h_2}{roi1_subs_factor + 8}\right)$$

For ROI 2, 3 and 4**:**

$$ROI_height = \mathrm{INT}\left(\frac{8 \times roiN_h}{roiN_subs_factor + 8}\right)$$

If (*roiN_binning_en* = 1 AND *color_en* = 0) OR (*roiN_binning_en* = 0 AND *color_en* = 1)

For ROI 1

$$ROI_height = 2 \times \left[\mathrm{INT}\left(\frac{4 \times roi1_h_1}{roi1_subs_factor + 8}\right) + \mathrm{INT}\left(\frac{4 \times roi1_h_2}{roi1_subs_factor + 8}\right)\right]$$

For ROI 2, 3 and 4**:**

$$ROI_height = 2 \times \mathrm{INT}\left(\frac{4 \times roiN_h}{roiN_subs_factor + 8}\right)$$

If *roiN_binning_en* = 1 AND *color_en* = 1

For ROI 1:

$$ROI_height = 4 \times \left[\mathrm{INT}\left(\frac{2 \times roi1_h_1}{roi1_subs_factor + 8}\right) + \mathrm{INT}\left(\frac{2 \times roi1_h_2}{roi1_subs_factor + 8}\right)\right]$$

For ROI 2, 3 and 4:

$$ROI_height = 4 \times \left[\mathrm{INT}\left(\frac{2 \times roiN_h}{roiN_subs_factor + 8}\right)\right]$$

Then, *height_out* is:

$$\rightarrow \quad height_out = \frac{ROI_height - 4 \times ddc_en}{2^{roiN_binning_en}}$$

Notes:

- INT( ) takes the integer part of the division result.
- N stands for ROI index (1, 2, 3 or 4).
- If defect correction is active, the minimum ROI size is 5; defect correction must be disabled for smaller ROI size.

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4.5.4 Multi-ROI

The multi-ROI offers two different and separate modes:

- **MIMR (Multiple Integration Multiple ROI) mode** allows the user to define an acquisition cycle comprising 1 to 4 ROI cycle(s) (see ***roi_max_id*** in **<reg_chain_cfg>** in Section 17.3.7).
- **SIMR (Single Integration Multiple ROI) mode** acts on the first ROI of the multi-ROI cycle only, allows 1, 2 or 4 areas of interest to be acquired within the same integrated image. In SIMR mode, the sensor outputs only the configured zones and concatenates them to form a single image (see Section 4.5.4.2).

Each ROI has its own specific parameters (see Table 4-2) and parameters that are common to all ROIs (see Table 4-3).

Table 4-2. ROI-specific parameters

Parameter	Description	Register bitfield names			
		ROI1	ROI2	ROI3	ROI4
ROI Configuration	Defines the ROI dimensions and position in the total field of view.	***roi1_0l_1*** ***roi1_h_1*** ***roi1_0c_1*** ***roi1_w_1*** ***roi1_0l_2*** ***roi1_h_2*** ***roi1_0c_2*** ***roi1_w_2*** in **<reg_roi1*>**, see Section 17.3.11	***roi2_0l_1*** ***roi2_h_1*** ***roi2_0c_1*** ***roi2_w_1*** in **<reg_roi2*>**, see Section 17.3.12	***roi3_0l_1*** ***roi3_h_1*** ***roi3_0c_1*** ***roi3_w_1*** in **<reg_roi3*>**, see Section 17.3.13	***roi4_0l_1*** ***roi4_h_1*** ***roi4_0c_1*** ***roi4_w_1*** in **<reg_roi4*>**, see Section 17.3.14
Integration times	For each ROI two integration times have to be defined, one in number of lines and one in sub-line times.	***roi1_t_int_ll*** ***roi1_t_int_clk*** in **<reg_roi1*>**, see Section 17.3.11	***roi2_t_int_ll*** ***roi2_t_int_clk*** in **<reg_roi2*>**, see Section 17.3.12	***roi3_t_int_ll*** ***roi3_t_int_clk*** in **<reg_roi3*>**, see Section 17.3.13	***roi4_t_int_ll*** ***roi4_t_int_clk*** in **<reg_roi4*>**, see Section 17.3.14
Analog and digital gains		***roi1_ana_gain*** ***roi1_dig_gain*** in **<reg_roi1*>**, see Section 17.3.11	***roi2_ana_gain*** ***roi2_dig_gain*** in **<reg_roi2*>**, see Section 17.3.12	***roi3_ana_gain*** ***roi3_dig_gain*** in **<reg_roi3*>**, see Section 17.3.13	***roi4_ana_gain*** ***roi4_dig_gain*** in **<reg_roi4*>**, see Section 17.3.14
Vertical and horizontal sub-sampling factors		***roi1_subs_v*** ***roi1_subs_h*** in **<reg_roi1*>**, see Section 17.3.11	***roi2_subs_v*** ***roi2_subs_h*** in **<reg_roi2*>**, see Section 17.3.12	***roi3_subs_v*** ***roi3_subs_h*** in **<reg_roi3*>**, see Section 17.3.13	***roi4_subs_v*** ***roi4_subs_h*** in **<reg_roi4*>**, see Section 17.3.14

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Table 4-2. ROI-specific parameters (Continued)

Parameter	Description	Register bitfield names			
		ROI1	ROI2	ROI3	ROI4
Binning factor	Binning is performed after the sub-sampling if this is used. Each ROI can have its own binning factor. See Section 9.	***roi1_binning_en*** in **<reg_chain_cfg>**, see Section 17.3.7	***roi2_binning_en*** in **<reg_chain_cfg>**, see Section 17.3.7	***roi3_binning_en*** in **<reg_chain_cfg>**, see Section 17.3.7	***roi4_binning_en*** in **<reg_chain_cfg>**, see Section 17.3.7
Repetition count	Each ROI will be repeated several times before reading the next ROI.	***roi1_rep_nb*** in **<reg_roi1*>**, see Section 17.3.11	***roi2_rep_nb*** in **<reg_roi2*>**, see Section 17.3.12	***roi3_rep_nb*** in **<reg_roi3*>**, see Section 17.3.13	***roi4_rep_nb*** in **<reg_roi4*>**, see Section 17.3.14
Wait time	Wait time after the end of the last ROI repetition (see Figure 4-7 Multi-ROI cycle).	***roi1_t_wait_ext*** in **<reg_roi1*>**, see Section 17.3.11	***roi2_t_wait_ext*** in **<reg_roi2*>**, see Section 17.3.12	***roi3_t_wait_ext*** in **<reg_roi3*>**, see Section 17.3.13	***roi4_t_wait_ext*** in **<reg_roi4*>**, see Section 17.3.14

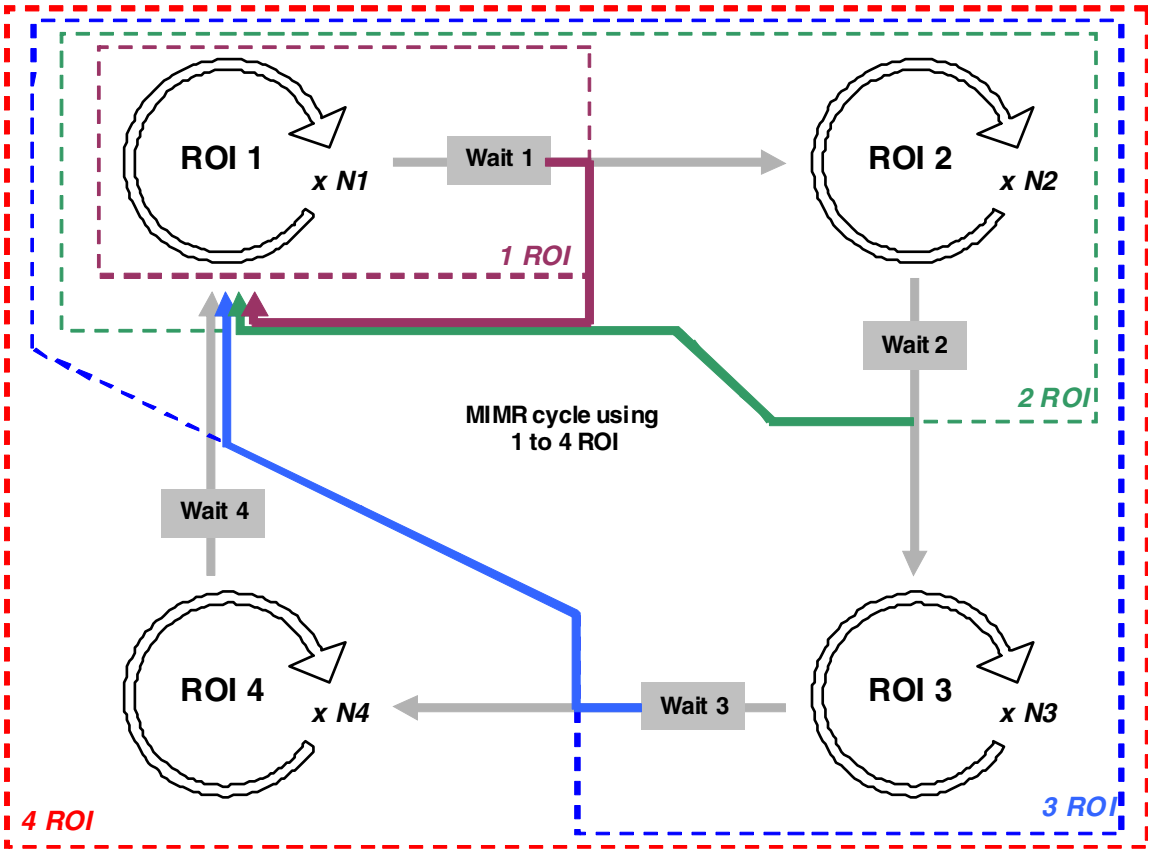
All the used ROIs use these common parameters:

Table 4-3. ROI common parameters

Parameter	Description	Register bitfield names
Binning factor divider	The binning result may be divided by 1, 2 or 4 to either keep the maximum amount of information or reduce the noise.	***binning_div_factor*** in **<reg_chain_cfg>**, see Section 17.3.7
Flip configuration	(see Figure 4-4: Flip effect)	***roi_flip_h*** and ***roi_flip_v*** in **<reg_miscel2>**, see Section 17.3.4
Readout mode		***roi_readout_mode*** , see Section 17.3.8
Digital color gains (For color sensor)		***gb_dig_gain***; ***gr_dig_gain***; in **<reg_dig_gain_gb_gr>,** see Section 17.3.16 ***b_dig_gain***; ***r_dig_gain*** in **<reg_dig_gain_b_r>**, see Section 17.3.15
Wait time at the end of each frame		***roi_t_wait***, see Section 17.3.10
Line length		***line_length***, see Section 17.3.1
Clamp configuration and offsets	Depends on MIMR, SIMR or High dynamic configuration. See Section 4.5.4.1, Section 4.5.4.2 and Section 4.5.4.3	

4.5.4.1 *Multiple Integration (MIMR) Mode Configuration*

Figure 4-7. Multi-ROI cycle in MIMR mode



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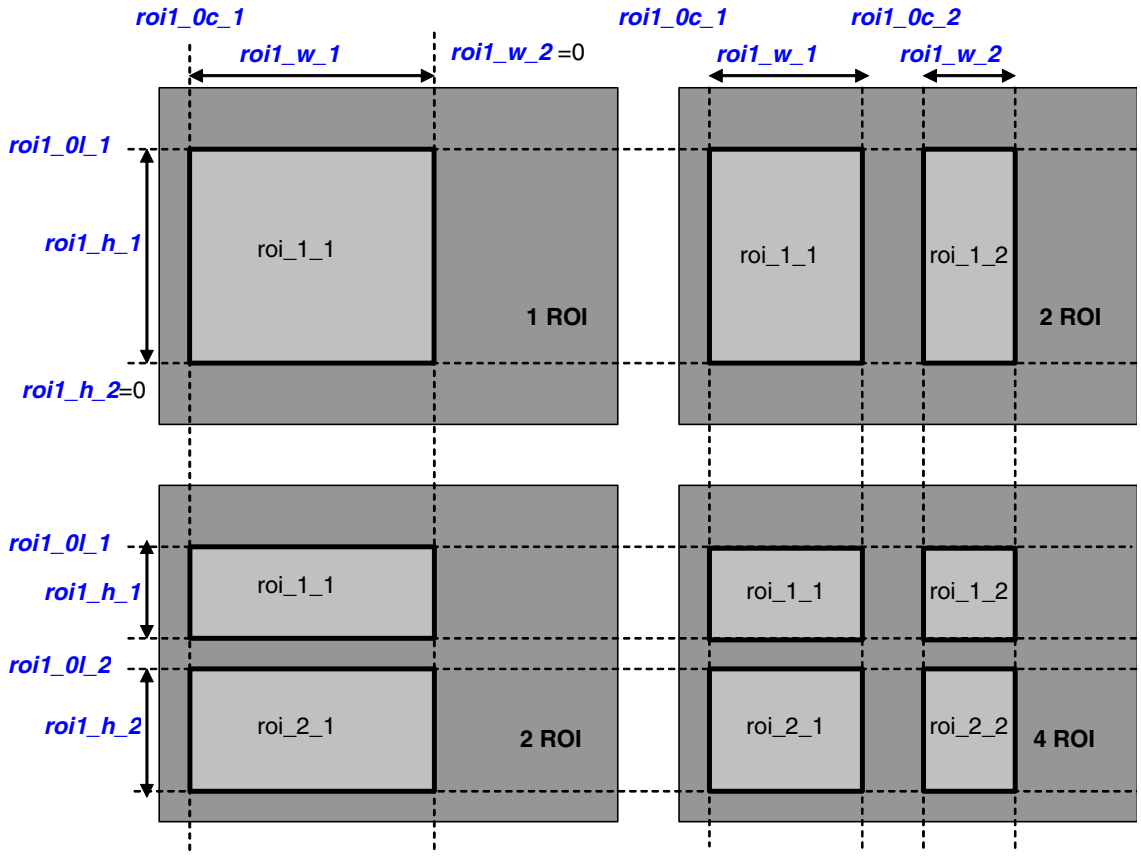
4.5.4.2 Single Integration (SIMR) Mode Configuration

Figure 4-8. SIMR parameters



All the ROI 1 registers are described in Section 17.3.11.

- If the ROI_1_2 width and ROI_2_1 height are null, only ROI_1_1 is read. The user has to choose:
  - ROI_1_1 horizontal (***roi1_0c_1***) and vertical (***roi1_0l_1***) offsets.
  - ROI_1_1 horizontal (***roi1_w_1***) and vertical (***roi1_h_1***) dimensions.
- If the ROI_1_2 width is greater than 0 and ROI_2_1 height is null, only ROI_1_1 and ROI_1_2 are read. The user has to choose:
  - ROI_1_1 horizontal (***roi1_0c_1***) and vertical (***roi1_0l_1***) offsets.
  - ROI_1_1 horizontal (***roi1_w_1***) and vertical (***roi1_h_1***) dimensions.
  - ROI_1_2 horizontal (***roi1_0c_2***) offset. (ROI_1_2 vertical offset = ROI_1_1).
  - Horizontal (***roi1_w_2***) width (ROI_1_2 height = ROI_1_1).
- If the ROI_1_2 width is null and ROI_2_1 height is greater than 0, only ROI_1_1 and ROI_2_1 are read. The user has to choose:
  - ROI_1_1 horizontal (***roi1_0c_1***) and vertical (***roi1_0l_1***) offsets.
  - ROI_1_1 horizontal (***roi1_w_1***) and vertical (***roi1_h_1***) dimensions.
  - ROI_2_1 vertical (***roi1_0l_2***) offset. (ROI_2_1 horizontal offset = ROI_1_1).

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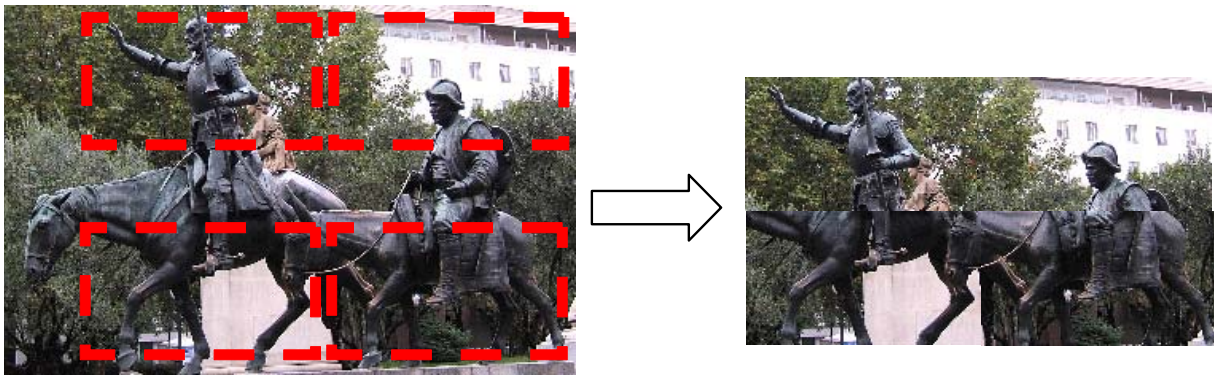
  - ROI_2_1 height (***roi1_h_2***) (ROI_2_1 width is the same as ROI_1_1).
- If the ROI_1_2 width and ROI_2_1 height are greater than 0, then 4 ROI_1_1, ROI_2_1, ROI_1_2 and ROI_2_2 are read. The user has to choose:
  - ROI_1_1 horizontal (***roi1_0c_1***) and vertical (***roi1_0l_1***) offsets.
  - ROI_1_1 horizontal (***roi1_w_1***) and vertical (***roi1_h_1***) dimensions.
  - ROI_2_1 ROI_2_2 vertical (***roi1_0l_2***) offset and (***roi1_h_1***) height.
  - ROI_1_2 horizontal (***roi1_0c_2***) offset and (***roi1_w_2***) width.

Figure 4-9. ROI output for the "4 ROI" configuration



When using the defect correction (***roi_ddc_en*** = 1) there is:

- A 4-column (or 2 if binning function is enabled) black border between ROI_1_1 and ROI_1_3 and ROI_1_2 and ROI_1_4.
- A 4-line (or 2 if binning function is enabled) black border between ROI_1_1 and ROI_1_2 and ROI_1_3 and ROI_1_4.

4.5.4.3 High Dynamic Range Configuration

A special MIMR configuration using two integration times can be used to provide high dynamic images.

The first integration time image followed by a second integration image can be combined out of the chip, without any image loss. For example:

- Image 1 with a short integration time
- Image 2 with N time longer integration time
- A computed image may be calculated by summing image 2 + [image 1 with each of its pixel values multiplied by N]

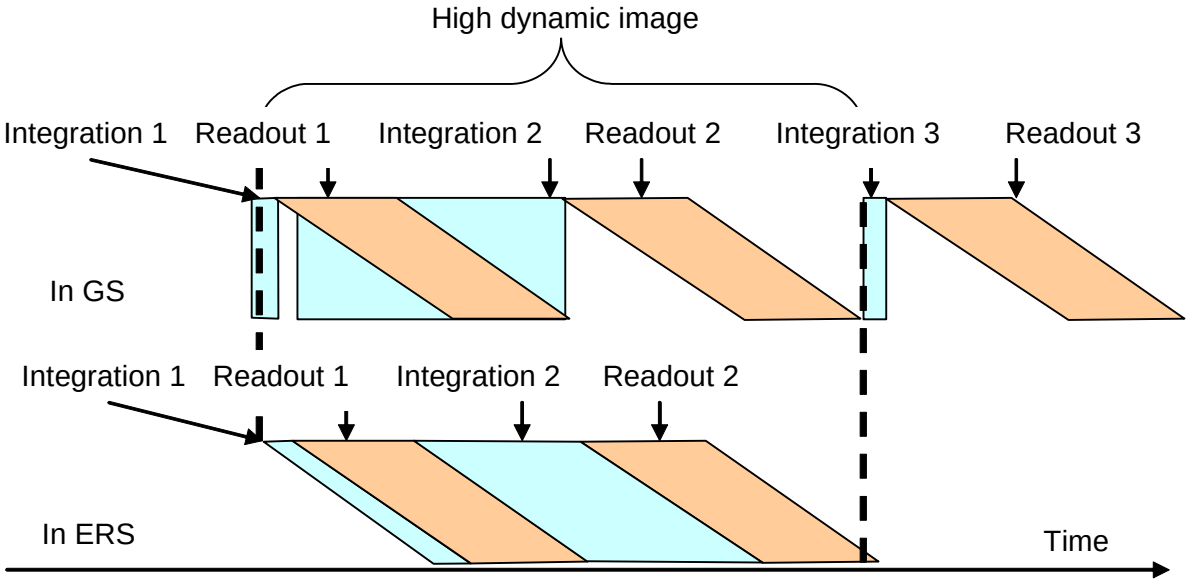
Note that due to the 60 fps maximum frame rate a true 30 fps output can be achieved.

In this mode only two ROIs are used. They must have the same:

- Position and dimensions.
- Binning
- Sub-sampling factor
- Repetition factor (=1)
- ROI mode (SIMR must not be used)

To prevent motion distortion it is recommended to perform the short integration time first.

Figure 4-10. Dual integration time mode for high dynamic



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5. 10-Bit ADC

5.1 Analog Gain

Digital conversion is done by a high speed 10-bit column ADC. All the pixel values of the same line are converted in parallel.

The analog gain is done by a slope adjustment. There are 8 available values. These values are programmable via SPI. Each ROI has its own analog gain:

- ***roi1_ana_gain*** in **<reg_roi1*>** for ROI 1 (see Section 17.3.11)
- ***roi2_ana_gain*** in **<reg_roi2*>** for ROI 2 (see Section 17.3.12)
- ***roi3_ana_gain*** in **<reg_roi3*>** for ROI 3 (see Section 17.3.13)
- ***roi4_ana_gain*** in **<reg_roi4*>** for ROI 4 (see Section 17.3.14)

5.2 External Resistor Choice

The ADC gain value is set through an external resistor connected between ADC_REF_1 and ADC_REF_2 pins. An internal protection against a short circuit between these two pins is included in the design.

$$R_{EXT} = \frac{K}{CLK_ADC} - 80$$

where K = 1.94×10^{12}, CLK_ADC is in Hertz and R_{EXT} is in Ohms.

With a 114 MHz ADC clock, the resistor value is 16.9 kΩ.

5.3 Analog Gain Tolerances

Table 5-1. ADC gain tolerances

1	1.5	2	3	4	6	8
89.09	59.09	44.18	29.64	22.30	14.90	11.27
Precision	0.5%	1%	1%	1%	1	2%

6. Clamp and Offset Adjustment

The purpose of the automatic black level adjustment function (or clamp) is to cancel:

- The offset due to pixel dark current (offset variable with temperature and integration time).
- The analog chain offset (mainly due to comparator offset).

The black level adjustment is active up to 65 °C with 200 ms integration time.

Black level adjustment can be automatic or manual. This is selected by the ***clamp_auto_en*** bit in the **<reg_miscel2>** register. See Section 17.3.4

In order to compensate possible differences in dark current generation between masked pixels and useful pixels, the automatic black level correction works as follows:

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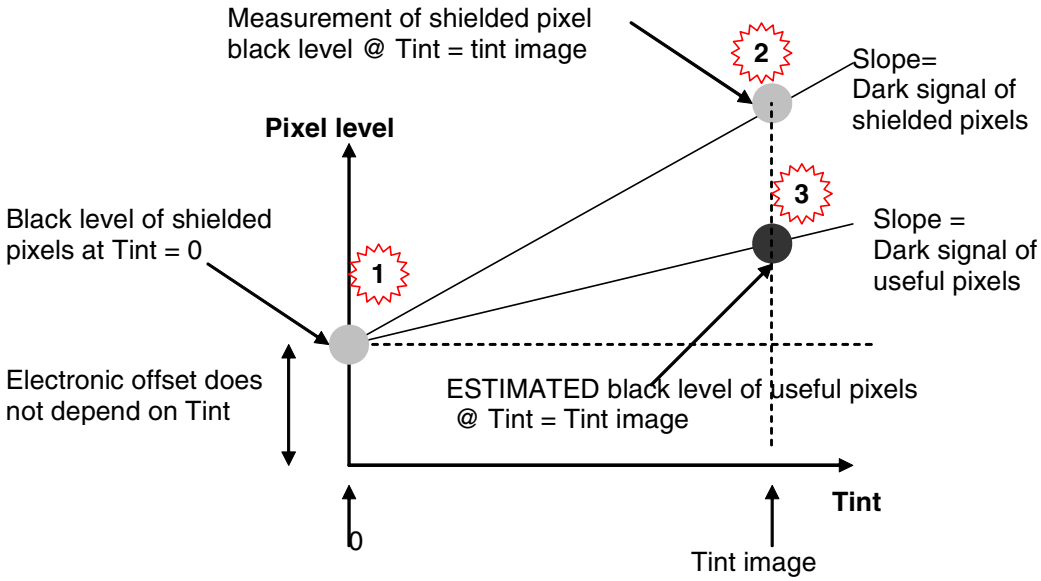
Figure 6-1. Clamp principle



For each frame acquisition:

1. A first measurement is taken on a shielded pixel with a very short integration time (fixed to the minimum possible time) to determine the hardware offset of the acquisition chain (chain_offset).
2. A second measurement is taken to determine the dark signal mean value of a shielded pixel for the configured integration time (shld_pix_level).
3. The dark signal of a useful pixel is deduced from these 2 measurements and from the ratio between useful and shielded pixels (V0_ratio). This ratio is configurable via the ***v0_gain*** bit field in the **<reg_clamp_cfg>** register. See Section 17.3.18.

$$\text{Useful dark signal} = (\text{shielded pixel level} - \text{chain offset}) \times \text{V0_ratio} + \text{chain offset}$$

A lock mechanism guarantees a constant correction offset as long as the difference between the new correction offset and the current correction is less than a threshold configurable by ***clamp_lock_th*** in **<reg_clamp_cfg>** see Section 17.3.18. This mechanism is necessary to ensure offset stability during a video stream. It can be bypassed using ***clamp_lock_en*** in **<reg_clamp_cfg>**, see Section 17.3.18.

Offset can be adjusted using either ***clamp_add_offset*** (if ***clamp_auto_en*** = '1' in **<reg_miscel2>**) or ***clamp_manual_offset*** (if ***clamp_auto_en*** = '0' in **<reg_miscel2>**) in **<reg_clamp_offset>**, see Section 17.3.17.

The ***flag_dig_cor*** flag in the **<fb_status>** register indicates if a digital correction is needed or not, see Section 17.3.23.

If the analog correction allowed by **<max_offset>** is saturated, a digital correction can be activated by setting **<dig_cor_en>**.

If **<dig_cor_en>** = 1 and analog offset is saturated, then the maximum data output level will be limited.

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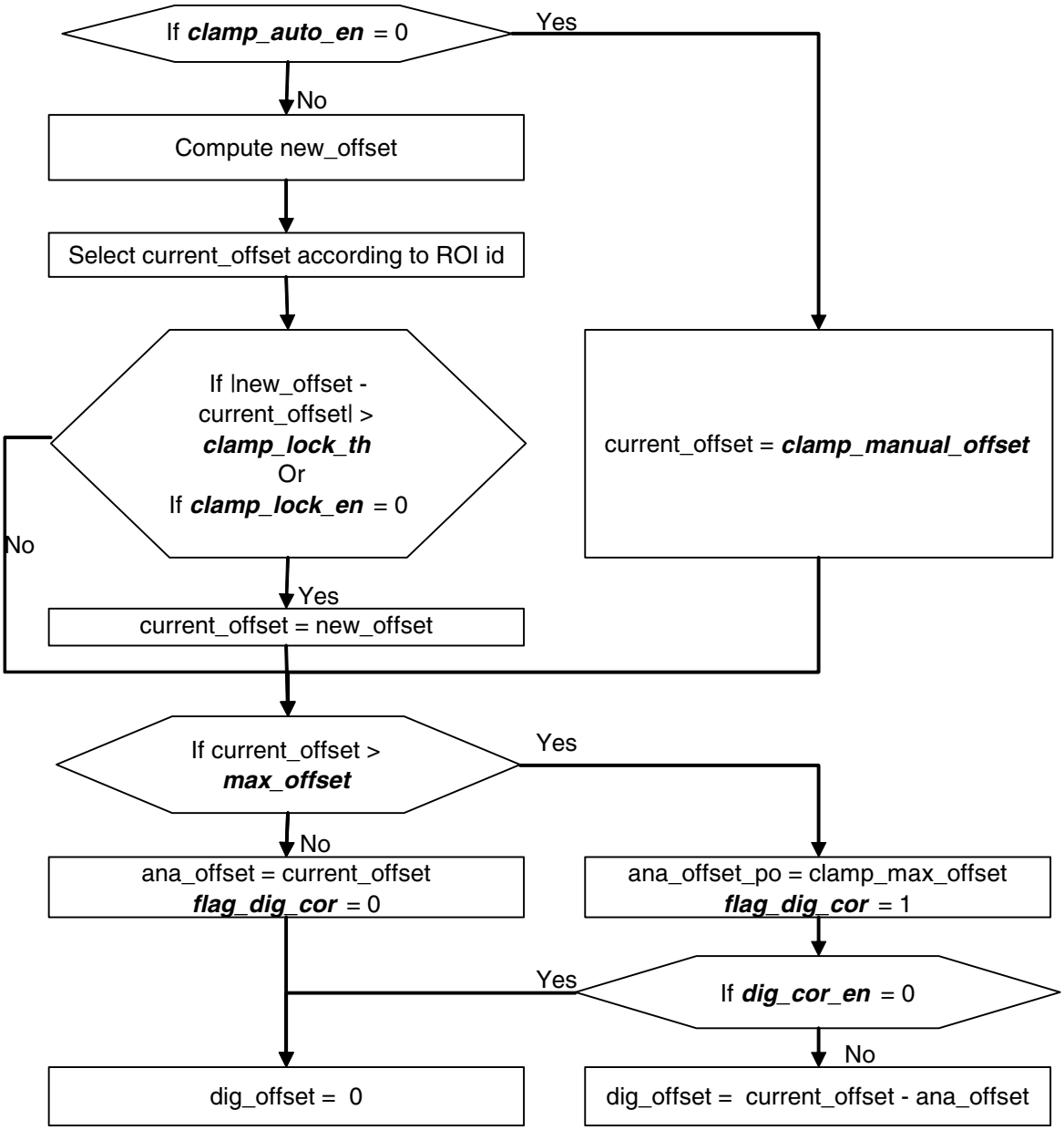
Digital and analog offsets are output in two feedback bitfields ***fb_ana_offset*** and ***fb_dig_offset*** in **<fb_clamp>**, see Section 17.3.22.

Figure 6-2. Clamp algorithm



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7. Digital Gain

This block applies one global gain followed by four digital gains (for the Bayer or 2x2 WRGB CFA structures) configurable by 8-bit SPI registers.

In B&W products, only the global gain is used.

To allow good precision with low gains the 8-bits for programming the digital gain are used as follows:

- The 2 MSB are used for precision P
- The 6 LSB are used to control the gain G (from 0 to 63)
- The ROIX digital gains (***roiX_dig_gain***) follow this rule:

$$Gain = 2^{P} \times \left(1 + \frac{G}{64}\right)$$

- For P=0 Gain varies from 1 to 1.98 in steps of 0.015
- For P=1 Gain varies from 2 to 3.97 in steps of 0.031
- For P=2 Gain varies from 4 to 7.94 in steps of 0.062
- For P=3 Gain varies from 8 to 15.88 in steps of 0.125

In color products, the four digital gains can be used to balance the four color channels (blue, green blue, green red and red):

- The 2 MSB are used for precision P
- The 6 LSB are used to control the gain G (from 0 to 63)
- The four digital color gains (***gb_dig_gain***; ***gr_dig_gain***; ***b_dig_gain***; ***r_dig_gain***) follow this rule:

$$Gain = 2^{P-2} \times \left(1 + \frac{G}{64}\right)$$

- For P=0 Gain varies from 0.25 to 0.5 in steps of 0.004
- For P=1 Gain varies from 0.5 to 0.99 in steps of 0.008
- For P=2 Gain varies from 1 to 1.98 in steps of 0.016
- For P=3 Gain varies from 2 to 3.97 in steps of 0.0.31

8. Defective Pixel Correction

A multidirectional 3x3 median filter (with maximal weighting) is implemented and can be enabled by programming ***roi_ddc_en*** in **< reg_chain_cfg >**. See Section 17.3.7.

This filter is compatible with B&W and color products (Bayer or WRGB). All pixels of the ROI are corrected; this correction deletes 2 pixels all around the input picture so the ROI output is reduced by 2 pixels in each line and column. See Section 4.5.3.

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9. Binning

Two binning 2x2 modes are implemented:

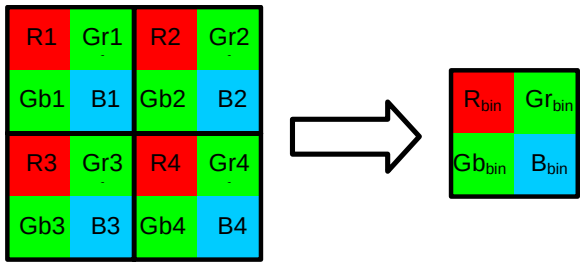
Figure 9-1. B&W binning (color_en=0)



$$P_{bin} = \frac{1}{k}\sum_{i=1}^{4} P_i$$

The k parameter, see ***binning_div_factor***, allows dividing the sum by 1, 2 or 4.

Figure 9-2. Color binning (color_en=1)



$$X_{bin} = \frac{1}{k}\sum_{i=1}^{4} X_i$$

With X = B, Gb, Gr or R.

The k parameter, see ***binning_div_factor***, allows dividing the sum by 1, 2 or 4.

The binning respects the Bayer pattern to add only the same color pixels.

When k= 4 → Average by 4 → Saturation remains the same and noise on the image is reduced by a factor 2.

When k=2 or 1, the sum is clipped at the value 1023.

The dimensions of the binning output image are half the input image dimensions.

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10. Histograms

Four histograms can be computed (for color sensors):

- The first one with green blue pixels
- The second one with red pixels
- The third one with blue pixels
- The fourth one with green red pixels

To enable histogram calculation program ***roi_histo_en*** in **< reg_chain_cfg>**, see Section 17.3.7.

The number of categories is selectable: 8, 16, 32 or 64 using ***hist_bin_nb*** in **<reg_chain_cfg>**. See Section 17.3.7.

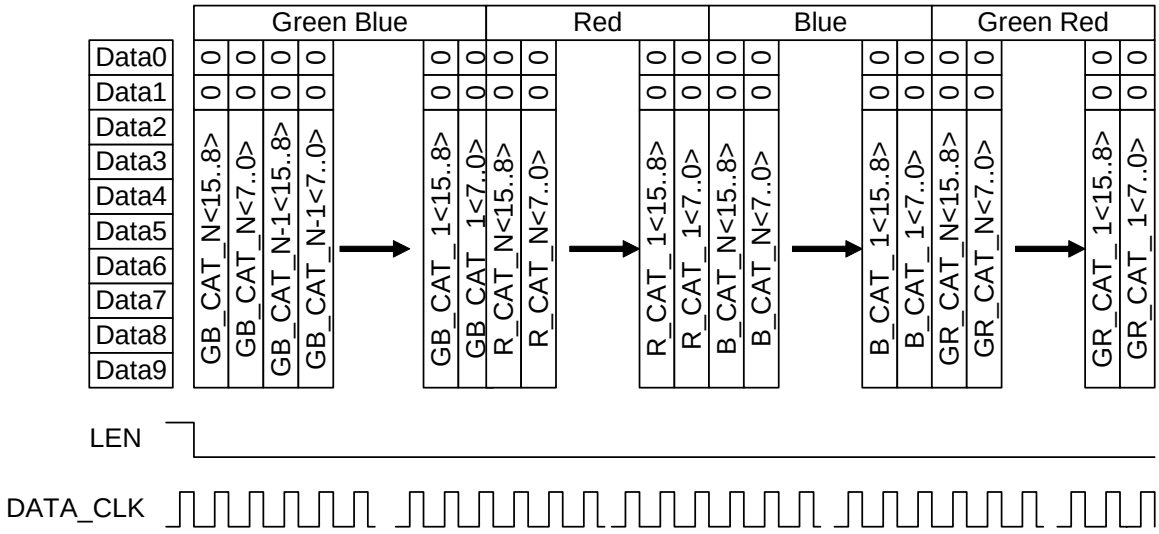
The histograms are output (see Figure 12-1 on page 27) with the number of bright pixels first.

Each category is coded on 16 bits and output on the 8 MSB of two successive pixels.

The 4 histograms are output serially without any delimiter.

The number of saturated pixels at zero and at 1023 are calculated and provided to the application in the footer. See Section 12.

Figure 10-1. Histogram outputs



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11. 10 to 8-Bit Compression

To allow the use of 8-bit output, the amplitude range is redefined with 256 levels.

8 data bits are output on the 8 MSB.

The transfer function is defined as follows:

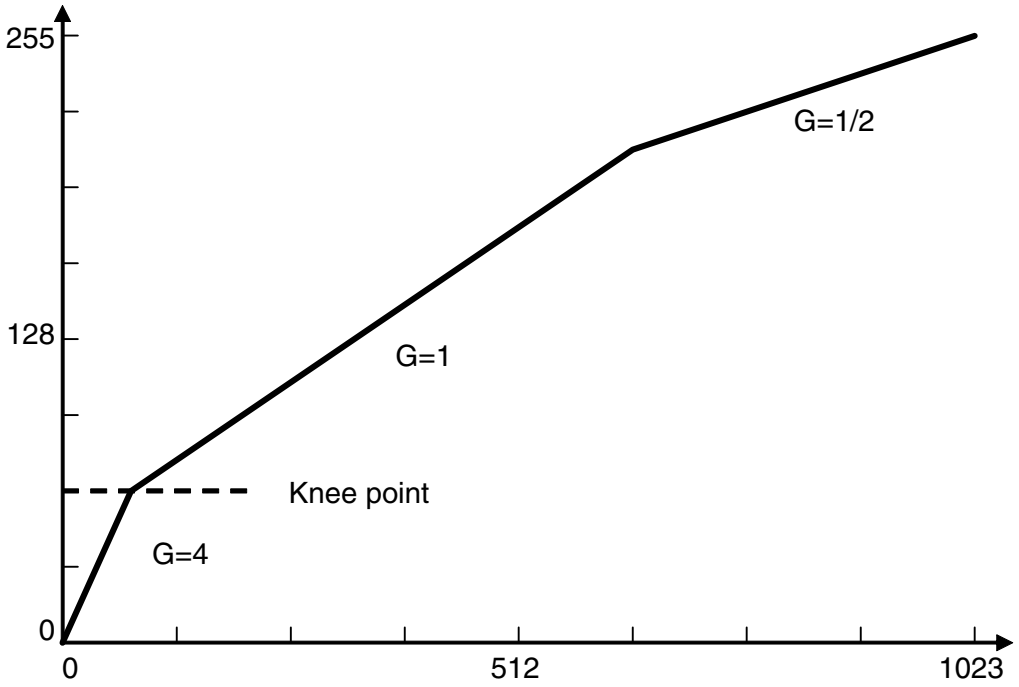
- The user has to choose the knee point KN by programming ***range_coeff*** in **<reg_miscel1>**.
- The output value on 8 bits follows these rules:

$$\text{For } 0 \le IN < K_N \longrightarrow OUT = IN$$

$$\text{For } K_N \le IN < 8 \bullet \left(128 - \frac{3}{4} K_N\right) \longrightarrow OUT = \frac{IN}{4} + \frac{3}{4}K_N$$

$$\text{For } 8 \bullet \left(128 - \frac{3}{4} K_N\right) \le IN < 1024 \longrightarrow OUT = \frac{IN}{8} + 128$$

Figure 11-1. 10 to 8 bit compression



To enable this function use ***range_en*** in **<reg_chain_cfg>** see Section 17.3.7.

Using a knee point at 0 will only output the 8 MSB of 10-bit values to the 8 MSB of the output without any compression.

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12. Context

This block inserts in the data stream the configuration of the sensor used for the current image.

Insertion image context is under SPI control. See ***roi_context_out_en*** in **<reg_chain_cfg>** in Section 17.3.7.

Each image has its own header and footer.

The context data may be output with or without a histogram output.

Context data are output on the first line and on the last line inside the FEN signal. The context is output as extra lines. If the stream is too long for the LEN (due to a small ROI) the output of the stream is not cut by the change of LEN state. This means that even for the context output the LEN duration is the same for the whole image comprising context and histograms.

Depending on ***mask_idle_data*** in **<reg_miscel2>** if the useful line length is too short, data may be truncated.

The data are output on the 8 MSB of the video output (the 2 LSB are left at 00).

Figure 12-1 shows the location of the header and histogram data in the final frame structure:

Figure 12-1. Header and histogram

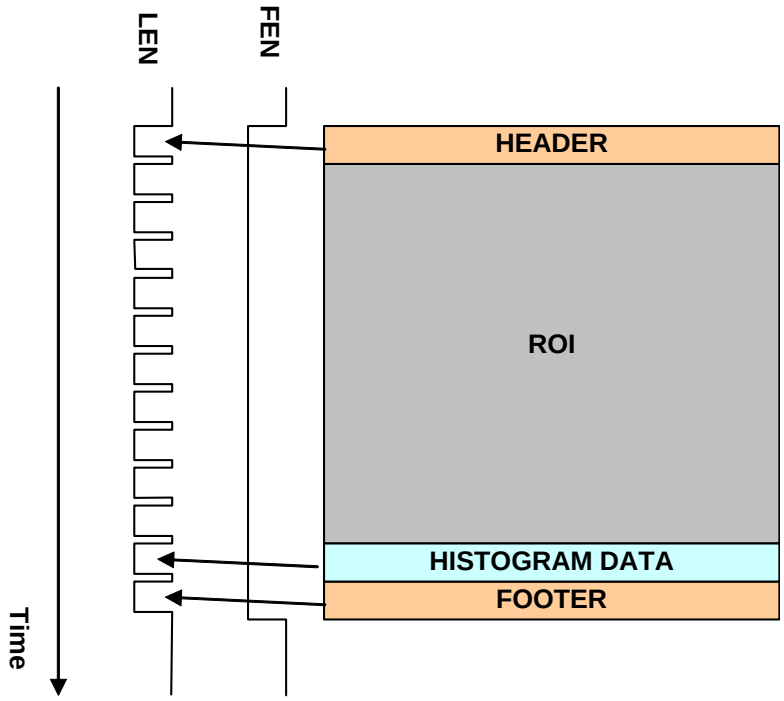

Table 12-1. Header content

Word count	Name	Description
0	"000000" & roi_id	ROI id (from 1 to 4)
1	roi_nb	ROI number (on 8-bit number of the readout image of this ROI)
2	"00000" & read_roi_0c_1[10:8]	Address of first column (MSB)
3	read_roi_0c_1[7:0]	Address of first column (LSB)

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Table 12-1. Header content (Continued)

Word count	Name	Description
4	"00000" & read_roi_0l_1[10:8]	Address of first line (MSB)
5	read_roi_0l_1[7:0]	Address of first line (LSB)
6	"00000" & roi_width[10:8]	ROI width (MSB)
7	roi_width[7:0]	ROI width (LSB)
8	"00000" & roi_height[10:8]	ROI Height (MSB)
9	roi_height[7:0]	ROI Height (LSB)
10	t_int_ll[15:8]	Main ROI integration time in line (MSB)
11	t_int_ll[7:0]	Main ROI integration time in line (LSB)
12	"00" & t_int_clk[13:8]	MSB of extra ROI integration time in CLK_CTRL × ***t_int_clk_mult_factor***
13	t_int_clk[7:0]	LSB of extra ROI integration time in CLK_CTRL × ***t_int_clk_mult_factor***
14	analog_gain	ROI analog gain
15	dig_gain_glob	ROI Global digital gain
16	dig_gain_b	Blue digital gain
17	dig_gain_gb	Green blue digital gain
18	dig_gain_gr	Green red digital gain
19	dig_gain_r	Red digital gain
20	fb_ana_offset	Analog offset
21	fb_dig_offset	Digital offset
22	'0'	(MSB)
	fb_flag_dir_cor	See Section 17.3.23
	fb_error_time_overflow	
	fb_error_corrupted_video	
	fb_error_ll_vs_xfer	
	fb_error_ll_vs_conv	
	fb_error_t_int_big	
	fb_error_t_int_small	(LSB)
23	t_frame_period_actual[15:8]	Frame period (MSB)
24	t_frame_period_actual [7:0]	Frame period (LSB)
	"00..0"	Line is filled with extra 00

Table 12-2. Footer content

Word count	Name	Description
0	'0'	See sensor status feedback Section 17.3.23.
	fb_flag_dir_cor	
	fb_error_time_overflow	
	fb_error_corrupted_video	
	fb_error_ll_vs_xfer	
	fb_error_ll_vs_conv	
	fb_error_t_int_big	
	fb_error_t_int_small	
1	low_sat_nb[15:8]	Number of pixels at 0 value (MSB)
2	low_sat_nb[7:0]	Number of pixels at 0 value (LSB)
3	high_sat_nb[15:8]	Number of pixels at 1023 value (MSB)
4	high_sat_nb[7:0]	Number of pixels at 1023 value (LSB)
	"00..0"	Line is filled with extra 00

13. Mux Out

This block multiplexes the different signals to the output: video, context and histograms.

14. Timing Generator and Power Management

Under SPI control, the timing generator provides the necessary timing to the sensor. It manages the different read modes depending on the global states programmed by the application. It times the reading of the matrix to follow the ROI, binning and sub-sampling functions.

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15. Clock Generator

The application has to provide 1 or 2 clocks to the sensor:

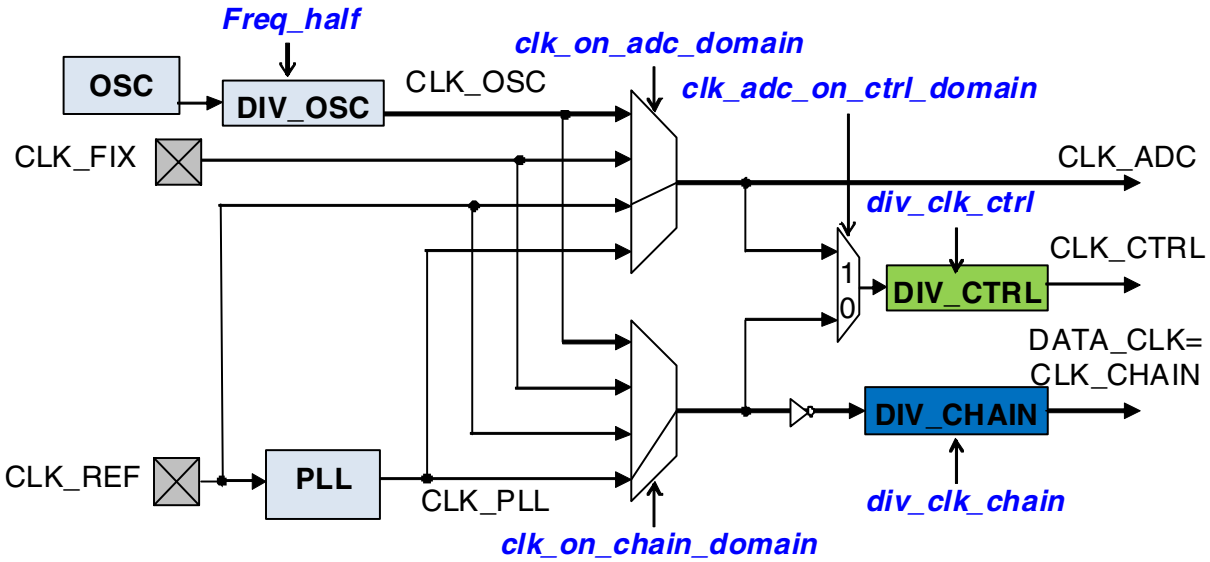
- The reference clock (CLK_REF).
- A second stable clock (CLK_FIX) if the application needs to dither CLK_REF to improve EMC performance.

Two other clocks are available in the sensor:

- CLK_OSC which is generated by an internal oscillator.
- CLK_PLL which is output by the PLL with CLK_REF as the reference clock.

These four clocks are the sensor input clocks.

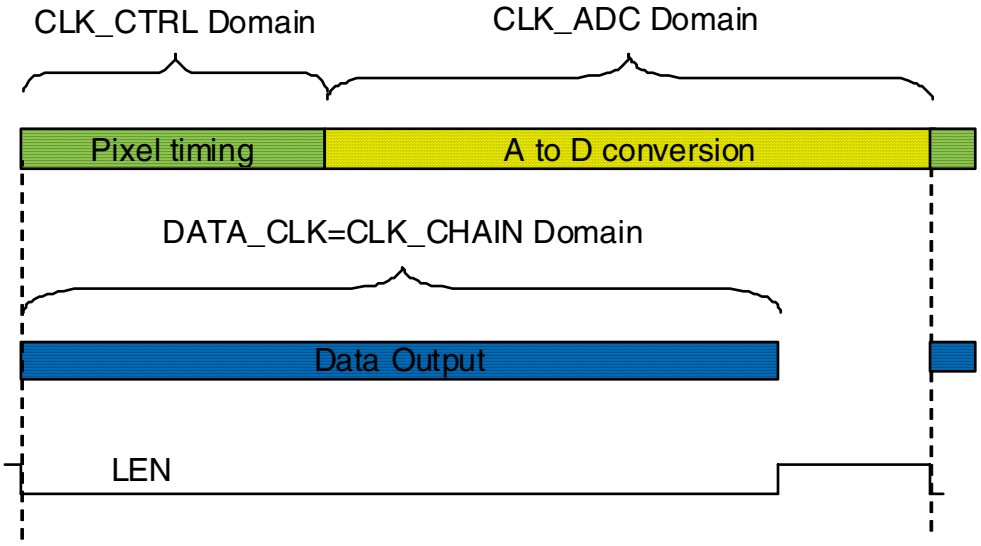
Figure 15-1. Clock management



The sensor needs three different clocks for three separate domains (See Figure 2-1: Block Diagram):

- One for the ADC (CLK_ADC).
- One for the timing control (CLK_CTRL).
- One for the digital chain (CLK_CHAIN).

Figure 15-2. Clock domains



Notes:

CLK_ADC and CLK_CTRL must be stable. Clock dithering is not allowed except for CLK CHAIN which may be dithered for EMC reasons if needed.

Pixel timing duration is given in Section 19.5.

A to D conversion and data output durations are computed in Section 19.4.

15.1 PLL

A Phase-Locked Loop block (PLL) is embedded to provide an output frequency (CLK_PLL) from a reference frequency (CLK_REF). The PLL supports a dithered CLK_REF. (See Figure 15-1: Clock management).

If the PLL is not used, the block is in power down mode.

15.1.1 Register used

pll_od, ***pll_n*** and ***pll_fb*** in **<Reg_pll_cfg>** see Section 17.3.6.

The PLL output frequency CLK_PLL is given by the equation:

$$CLK_PLL = \frac{M}{N \times P} \times CLK_REF$$

With:

4 < M =2x(pll_fb + 1) < 512,

2 < N =2x(pll_n + 1) < 20,

P (pll_od+1) = 4

5 MHz < CLK_REF < 50 MHz.

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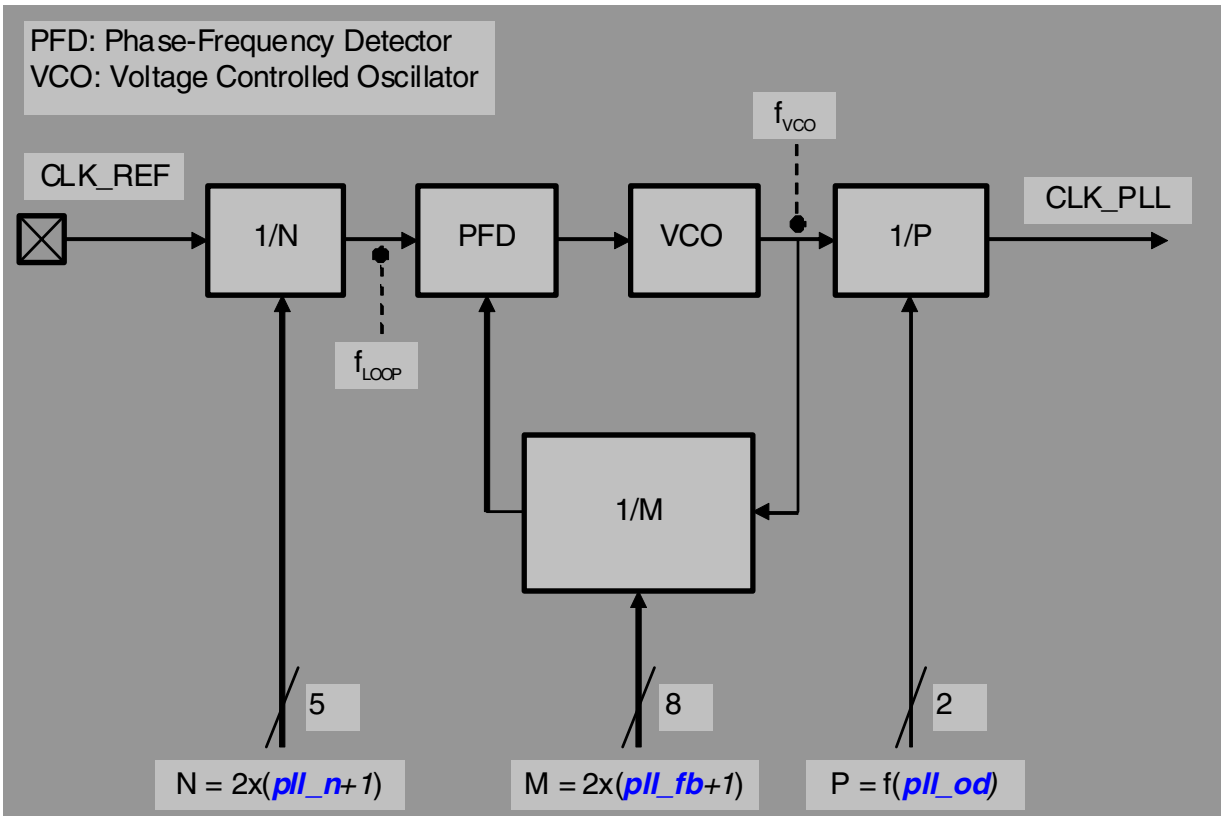
Figure 15-3. PLL block diagram



15.1.2 Limits and Conditions

The following conditions and limits must be respected to allow the PLL to operate efficiently:

- 325 MHz < f_{VCO} = CLK_PLL × P < 480 MHz
- 2.5 MHz < f_{LOOP}
- 81.25 MHz < CLK_PLL < 120 MHz

15.1.3 PLL Factor Calculations

For a given input frequency (CLK_REF) and the desired output frequency (CLK_PLL), follow these steps to calculate the pll_fb, pll_n and pll_od parameters.

1. Calculation of pll_od:
   – pll_od = P-1 = 3
2. Calculation of pll_n:

$$pll_n = \left(IntegerPart\left(\frac{CLK_REF}{5} \right) \right) \times 2 - 1$$

3. Calculation of pll_fb:

$$pll_fb = 2 \times RoundedUp\left(\frac{(pll_n+1) \times CLK_PLL \times (pll\ +od+1)}{CLK_REF} \right) -1$$

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4. Calculation of the PLL output frequency:

   The above formulas can be used to calculate the PLL output frequency (CLK_PLL).

The following table gives the some frequency calculation examples showing the P,N and M parameter settings used to obtain a 114 MHz system frequency with different input reference frequencies. The VCO frequency is 456 MHz.

Table 15-1. Example of PLL parameter settings to obtain 114 MHz CLK_PLL output frequency

Parameter settings	CLK_REF input frequency		
	12 MHz	24 MHz	48 MHz
P	4	4	4
pll_od	h03	h03	h03
N	4	8	18
pll_n	h01	h03	h08
M	152	152	172
pll_fb	h4B	h4B	h55

15.2 Internal Oscillator

The internal oscillator has to be calibrated by the application. During the calibration procedure the sensor counts the number of CLK_OSC cycles during the calibration reference period ***calib_count_ref***. The length of ***calib_count_ref*** is defined by the user as a number of CLK_REF cycles. The number of CLK_OSC cycles can be read in the ***fb_calib_count_osc*** register when the ***flag_reg_calib_count_ref*** flag goes back to low level.

If needed the oscillator frequency can be adjusted using ***prg_osc_freq_adjust*** in **<reg_prg_osc>** see Section 17.3.19.

<freq_half> may be used to divide the internal oscillator frequency by 2.

The internal oscillator frequency can be computed using the formula below, where R_{EXT} is the ADC_REF external resistor:

$$\text{Frequency} = \frac{1}{\left[\frac{R_{EXT} \times 316\ (10^{-13})}{36 + \text{prg_osc_freq_adjust}}\right] + 3.4\ (10^{-9})}$$

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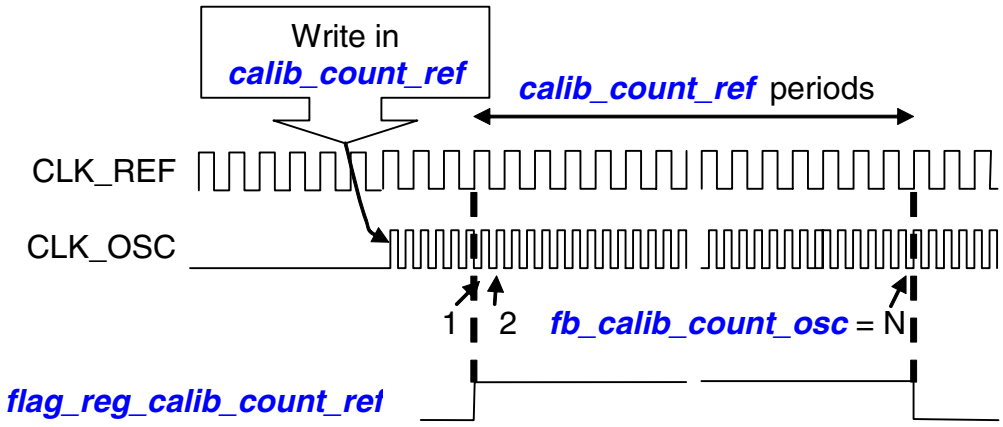
Figure 15-4. Oscillator calibration



15.3 Nominal Clock Configurations

CLK_OSC is used for A to D conversion (CLK_ADC) and pixel timing (CLK_CTRL) with a DIV_CTRL = 2

CLK_PLL is used for the digital chain (CLK_CHAIN).

The typical clock configuration is as follows:

clk_on_adc_domain = h2 in **<reg_clk_cfg>** see Section 17.3.5

clk_on_ctrl_domain = h1 in **<reg_clk_cfg>** see Section 17.3.5

clk_on_chain_domain = h3 in **<reg_clk_cfg>** see Section 17.3.5

div_clk_chain = h2 in **<reg_clk_cfg>** see Section 17.3.5

With this configuration a dithered clock can be used as CLK_REF for the PLL.

To allow the maximum frame rate, CLK_OSC must be above 114 MHz.

16. Test Pattern Generator

A test pattern allows the signal processing to be checked. It generates repeated slope from 0 to 1023 with a 1 LSB step.

The timing and image size used in this mode uses the ROI and timing configuration.

The block generates 3 different patterns.

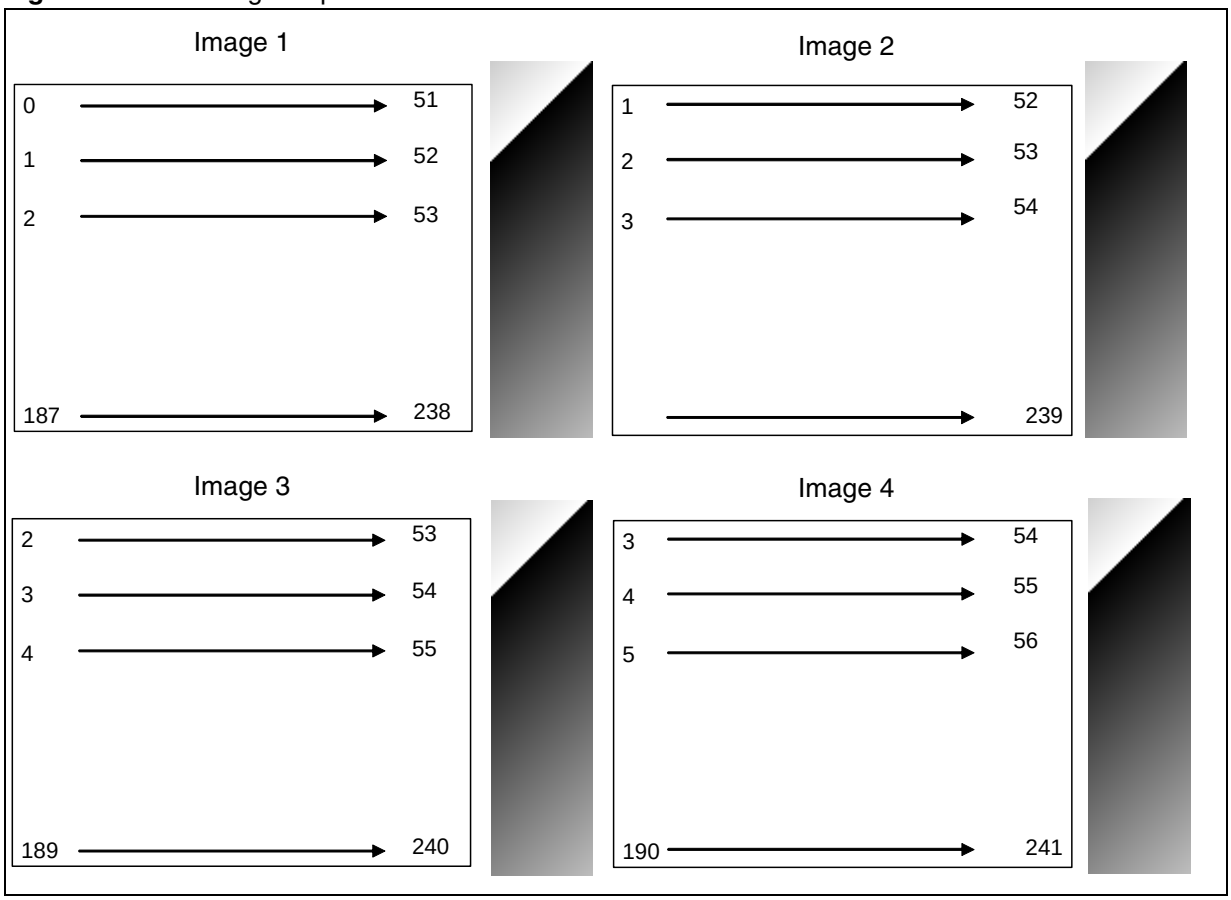
16.1 Moving Test Pattern

pattern_type = 01

In this mode, the test pattern changes from line to line and from frame to frame.

Figure 16-1 gives examples for a ROI (52 × 188 pixels). If the ROI width or height is larger than 1024 the test pattern counter will create additional ramp pulses in both directions.

Figure 16-1. Moving test pattern



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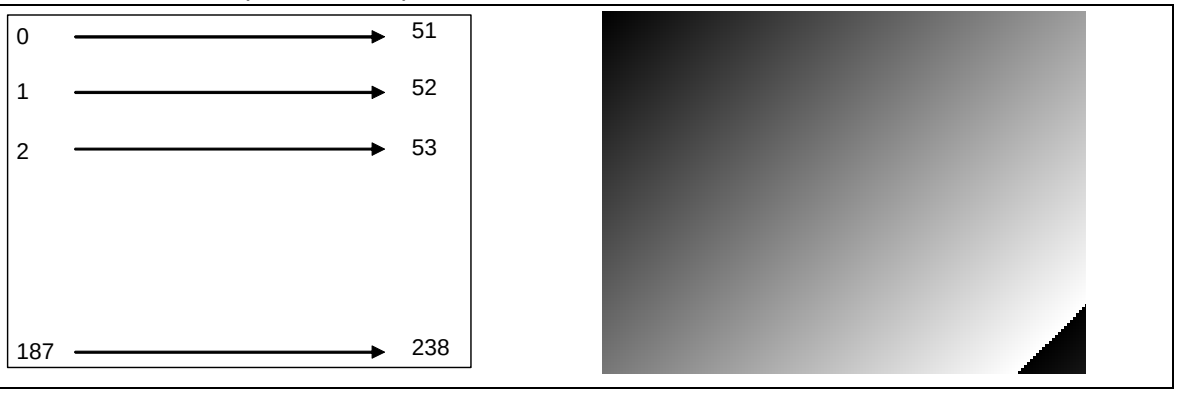
16.2 Fixed Test Pattern

pattern_type = 10

Figure 16-2 shows this pattern, using the same resolution as the previous example. The test pattern ramp generator will always have the same starting point at 0, at the first pixel of the first line.

Figure 16-2. Fixed test pattern example



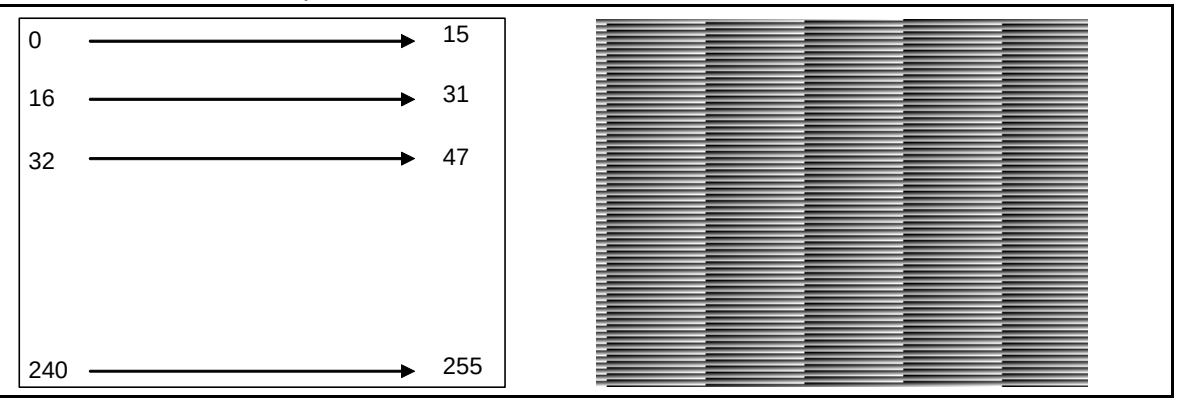
16.3 Functional Test Pattern

pattern_type = 11

This test pattern allows all output values to occur in the smallest possible image. The test pattern counter counts only during active FEN and LEN. The first pixel of the first line is at 0.

Figure 16-3 gives an example of a 16 × 16 image.

Figure 16-3. Functional test pattern



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17. SPI

The SPI communication interface allows the sensor to be controlled by an external device (SPI mode 0).

Most built-in functions are configurable via SPI registers. We can distinguish 6 types of registers:

- Dynamic registers (D) are read/write registers. They are refreshed only one time per frame at the beginning of the readout or on matrix reset, depending on the selected readout mode. A lock mechanism allows the refresh to be disabled. This is useful for ensuring that several register changes are taken into account in the same frame.
- Mailbox registers (MBX) are read/write registers. They are used to send abort requests or read calibration status information.
- Reset registers (RST) are read/write registers.They are used to perform a soft reset of the device.
- Static registers (S) are read/write registers. Any change in their value is taken into account immediately.
- Restricted static registers (RS) are like static registers but they must be modified only in STANDBY or IDLE state. Any change in their value during an acquisition sequence may have an unpredictable effect.
- Feedback registers (F) are read only registers. They are used to report the current state of the sensor.

17.1 Register Summary Tables

Table 17-1. 8-bit registers

Addr (hex)	Register Name	Type	Width	Bit	Content	Reference section	
0000	reg0	rs	8	7:0	Burst mode	Section 17.2.1	Section 17.4
0001	reg_soft_reset	rst	8	7:0	Soft reset global command	Section 17.2.2	
0002	calib_mbx	mbx	1	0	flag_reg_calib_count_ref	Section 17.2.3	
0003	abort_mbx	mbx	1	0	flag_abort_mbx	Section 17.2.4	

Table 17-2. 16-bit registers

Addr (hex)	Register Name	Type	Width	Bit	Content	Reference section	
0004	reg_line_cfg	rs	4	15:12	extra_line_nb	Section 17.3.1	
			1	11	Reserved		
			11	10:0	line_length		
0005	reg_flash_delay	rs	8	15:8	t_flash_del_off	Section 17.3.2	Section 19.6
			8	7 :0	t_flash_del_on		

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Table 17-2. 16-bit registers (Continued)

Addr (hex)	Register Name	Type	Width	Bit	Content	Reference section	
0006	reg_miscel1	rs	8	15:8	max_offset		
			8	7:0	range_coeff		Section 11.
0007	reg_miscel2	rs	1	15	reserved	Section 17.3.4	
			1	14	sync_flo_inv		Section 19.6
			1	13	sync_len_inv		
			1	12	sync_fen_inv		
			1	11	mask_idle_data		
			1	10	color_en		
			1	9	clamp_auto_en		Section 6.
			1	8	roi_expanded		
			1	7	roi_flip_h		Section 4.5.1
			1	6	roi_flip_v		
			2	5:4	pattern_type		Section 16.
			4	3:0	vlr_ph_ctrl		
0008	reg_clk_cfg	rs	1	15	clk_chain_low_pwr	Section 17.3.5	
			1	14	clk_out_inv		
			1	13	freq_half		
			1	12	clk _on_ctrl_domain		Section 15.
			2	11:10	clk_on_adc_domain		
			2	9:8	clk_on_chain_domain		
			4	7:4	div_clk_ctrl		
			4	3:0	div_clk_chain		
0009	reg_pll_cfg	rs	2	14:13	pll_od	Section 17.3.6	Section 15.1
			5	12:8	pll_n		
			8	7:0	pll_fb		

Table 17-2. 16-bit registers (Continued)

Addr (hex)	Register Name	Type	Width	Bit	Content	Reference section	
000A	reg_chain_cfg	d	2	15:14	t_int_clk_mult_factor	Section 17.3.7	
			2	13:12	roi_max_id		Section 4.5.4
			2	11:10	hist_bin_nb		Section 10.
			2	9:8	binning_div_factor		Section 9.
			1	7	roi_context_out_en		Section 12.
			1	6	roi_histo_en		
			1	5	roi_ddc_en		Section 8.
			1	4	range_en		Section 11.
			1	3	roi4_binning_en		Section 4.5.3
			1	2	roi3_binning_en		
			1	1	roi2_binning_en		
			1	0	roi1_binning_en		
000B	reg_ctrl_cfg	rs	1	13	dum_stdby_en	Section 17.3.8	
			1	12	dum_pwrup_en		
			1	11	dum_img_out_en		
			1	10	lock_dyn_reg		
			1	9	trig_pad_inv		
			1	8	trig_pad_sel		
			2	7:6	roi_flash_mode		Section 19.6
			2	5:4	roi_readout_mode		Section 18.2
			1	3	roi_video_en		Section 18.2.5
			1	2	roi_overlap_en		Section 18.2
			1	1	trig_rqst		
			1	0	stdby_rqst		Section 18.1.2
000C	reg_t_frame_period	d	16	15:0	t_frame_period	Section 17.3.9	
000D	reg_t_wait	d	16	15:0	t_wait	Section 17.3.10	

Table 17-2. 16-bit registers (Continued)

Addr (hex)	Register Name	Type	Width	Bit	Content	Reference section	
000E	reg_roi1_t_int_ll	d	16	15:0	roi1_t_int_ll	Section 17.3.11	Section 4.5.4
000F	reg_roi1_rep_nb_t_int_clk	d	8	15:8	roi1_rep_nb		
			8	7:0	roi1_t_int_clk		
0010	reg_roi1_t_wait_ext	d	11	10:0	roi1_t_wait_ext		
0011	reg_roi1_gain	d	3	10:8	roi1_ana_gain		
			8	7:0	roi1_dig_gain		
0012	reg_roi1_0l_1	d	11	10:0	roi1_0l_1		
0013	reg_roi1_h_1	d	11	10:0	roi1_h_1		
0014	reg_roi1_0c_1	d	11	10:0	roi1_0c_1		
0015	reg_roi1_w_1	d	11	10:0	roi1_w_1		
0016	reg_roi1_0l_2	d	11	10:0	roi1_0l_2		
0017	reg_roi1_h_2	d	11	10:0	roi1_h_2		
0018	reg_roi1_0c_2	d	11	10:0	roi1_0c_2		
0019	reg_roi1_w_2	d	11	10:0	roi1_w_2		
001A	reg_roi1_subs	d	8	15:8	roi1_subs_v		Section 4.5.3
			8	7:0	roi1_subs_h		
001B	reg_roi2_t_int_ll	d	16	15:0	roi2_t_int_ll	Section 17.3.12	Section 4.5.4
001C	reg_roi2_rep_nb_t_int_clk	d	8	15:8	roi2_rep_nb		
			8	7:0	roi2_t_int_clk		
001D	reg_roi2_t_wait_ext	d	11	10:0	roi2_t_wait_ext		
001E	reg_roi2_gain	d	3	10:8	roi2_ana_gain		
			8	7:0	roi2_dig_gain		
001F	reg_roi2_0l_1	d	11	10:0	roi2_0l_1		
0020	reg_roi2_h_1	d	11	10:0	roi2_h_1		
0021	reg_roi2_0c_1	d	11	10:0	roi2_0c_1		
0022	reg_roi2_w_1	d	11	10:0	roi2_w_1		
0023	reg_roi2_subs	d	8	15:8	roi2_subs_v		Section 4.5.3
			8	7:0	roi2_subs_h		

Table 17-2. 16-bit registers (Continued)

Addr (hex)	Register Name	Type	Width	Bit	Content	Reference section	
0024	reg_roi3_t_int_ll	d	16	15:0	roi3_t_int_ll	Section 17.3.13	Section 4.5.4
0025	reg_roi3_rep_nb_t_int_clk	d	8	15:8	roi3_rep_nb		
			8	7:0	roi3_t_int_clk		
0026	reg_roi3_t_wait_ext	d	11	10:0	roi3_t_wait_ext		
0027	reg_roi3_gain	d	3	10:8	roi3_ana_gain		
			8	7:0	roi3_dig_gain		
0028	reg_roi3_0l_1	d	11	10:0	roi3_0l_1		
0029	reg_roi3_h_1	d	11	10:0	roi3_h_1		
002A	reg_roi3_0c_1	d	11	10:0	roi3_0c_1		
002B	reg_roi3_w_1	d	11	10:0	roi3_w_1		
002C	reg_roi3_subs	d	8	15:8	roi3_subs_v		Section 4.5.3
			8	7:0	roi3_subs_h		
002D	reg_roi4_t_int_ll	d	16	15:0	roi4_t_int_ll	Section 17.3.14	Section 4.5.4
002E	reg_roi4_rep_nb_t_int_clk	d	8	15:8	roi4_rep_nb		
			8	7:0	roi4_t_int_clk		
002F	reg_roi4_t_wait_ext	d	11	10:0	roi4_t_wait_ext		
0030	reg_roi4_gain	d	3	10:8	roi4_ana_gain		
			8	7:0	roi4_dig_gain		
0031	reg_roi4_0l_1	d	11	10:0	roi4_0l_1		
0032	reg_roi4_h_1	d	11	10:0	roi4_h_1		
0033	reg_roi4_0c_1	d	11	10:0	roi4_0c_1		
0034	reg_roi4_w_1	d	11	10:0	roi4_w_1		
0035	reg_roi4_subs	d	8	15:8	roi4_subs_v		Section 4.5.3
			8	7:0	roi4_subs_h		
0036	reg_dig_gain_gb_gr	d	8	15:8	gb_dig_gain	Section 17.3.15	9
			8	7:0	gr_dig_gain		
0037	reg_dig_gain_b_r	d	8	15:8	b_dig_gain	Section 17.3.16	
			8	7:0	r_dig_gain		
0038	reg_clamp_offset	d	8	15:8	clamp_add_offset	Section 17.3.17	
			8	7:0	clamp_manual_offset		
0039	reg_clamp_cfg	rs	3	14:12	init_line_nb	Section 17.3.18	
			4	11:8	clamp_lock_th		
			1	7	clamp_lock_en		
			1	6	dig_cor_en		
			6	5:0	v0_gain		

Table 17-2. 16-bit registers (Continued)

Addr (hex)	Register Name	Type	Width	Bit	Content	Reference section	
003A	reg_prg_osc	rs	7	15:9	prg_osc_vsat_adjust	Section 17.3.19	
			2	8:7	prg_osc_vsat_select		
			7	6:0	prg_osc_freq_adjust		
003B	reg_calib_count_ref	rs	16	15:0	calib_count_ref	Section 17.3.20	
003C	fb_calib_osc_count	f	16	15:0	fb_calib_count_osc	Section 17.3.21	
003D	fb_clamp	f	8	15:8	fb_ana_offset	Section 17.3.22	
			8	7:0	fb_dig_offset		
003E	fb_status	f	1	8	flag_dig_cor	Section 17.3.23	
			2	7:6	fb_state_main_global		
			1	5	error_time_overflow		
			1	4	error_corrupted_video		
			1	3	error_ll_vs_xfer		
			1	2	error_ll_vs_conv		
			1	1	error_t_int_big		
			1	0	error_t_int_small		
003F to 0048	reserved						
0044	DATA_CLK activity	rs	1	13	*clk_out_low_pwr*	Section 17.3.24	
0049	pixtime_read_width	rs	8	15:8	pixtime_read_5t_width	Section 17.3.25	
			8	7:0	pixtime_read_4t_width		
7F	Chip_ID	f	16	15:0	Chip ID		

17.2 8-Bit Register Descriptions

17.2.1 Register 0

Name	reg0
Address	h00
Type	Restricted static
Default	h01

Default Value	Bitfield name	Description
0000 0001	*reg0_0[7:0]*	Master clock divider: 0➔ Normal mode active (no burst**)** 1➔ Burst mode active

17.2.2 Soft Reset Register

Name	reg_soft_reset
Address	h01
Type	Reset
Default	h00

Default Value	Bitfield name	Description
0000 0000	*soft_reset[7:0]*	Soft reset Writing or reading in SPI address h01 resets the whole chip, except the SPI state machine

17.2.3 Calibration Mailbox

Name	calib_mbx
Address	h02
Type	Mailbox
Default	h00

Default Value	Bitfield name	Description
0000 0000	*flag_reg_calib_count_ref*	Oscillator calibration status **0➔ Calibration sequence has ended (or not requested)** 1➔ Request was recorded. Calibration is ongoing. See reg_calib_count_ref in Section 17.3.20.

17.2.4 Abort Mailbox

Name	abort_mbx
Address	h03
Type	Mailbox
Default	h00

Default Value	Bitfield name	Description
0000 0000	*flag_abort_mbx*	Abort request / Abort status A write access to flag_abort_mbx generates an abort request. A read access returns the following status. **0➔** Abort has ended (or not requested) 1➔ Request was recorded. Current sequence should stop within one line duration. The abort action is requested by a single write to the flag_abort_mbx register itself.

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17.3 16-Bit Register Descriptions

17.3.1 Line Configuration

Name	reg_line_cfg
Address	h04
Type	Restricted static
Default	h8070

Default Value	Bitfield name	Description
1000 ---- ---- ---- ----	*extra_line_nb[15:12]*	Number of extra lines Defines the number of extra lines added after ROI readout Min = 0 ➔ 1 line added **Default = h8 ➔ 9 lines added** Max = hF ➔ d16 lines added See Section 19.2.2.
---- 0--- ---- ---- ----	*reserved*	
---- -000 0111 0000	*line_length[10:0]*	Line length Defines the line length specified in CLK_CTRL cycles multiplied by 8 (timing examples below with CLK_CTRL = 57 MHz). Section 19.4 - Line length calculation. Min = 0 **Default = h70 ➔ 15.72 µs** Max = h7FF ➔ 287 µs

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17.3.2 Flash Delay

Name	reg_flash_delay
Address	h05
Type	Restricted static
Default	h0000

Default Value	Bitfield name	Description
0000 0000 ---- ----	*t_flash_del_off[7:0]*	Flash off delay Delay between end of active FLO and end of integration specified in 8 × 1 line. Min = 0 ➔No delay added Max = hFF ➔ 255 × 8 = 2040 lines delay Note: t_flash_del_off must be lower than roi<i>_t_int_ll (ex: @ h0E for ROI1).
---- ---- 0000 0000	*t_flash_del_on[7:0]*	Flash on delay Delay between start of active FLO and start of integration specified in 8 × 1 line. Min = 0 ➔No delay added Max = hFF ➔ 255 × 8 = 2040 lines delay Note: 1. t_flash_del_on increases the frame period if roi_overlap_en (@ h0B) = 0. 2. If roi_readout_mode (@ h0B) = 4T ERS, the applied delay will be the programmed delay + 2 lines.

- Both flash delays are automatically set to 0 if roi_flash_mode (@ h0B) = 0 (= FLASH_OFF).
- t_flash_del_off is ignored if roi_flash_mode (@ h0B) = 3 (= FLASH_ON).
- t_flash_del_off should be set to 0 if roi_readout_mode (@ h0B) = 4T+ERS and roi_overlap_en (@ h0B) = 1. (If not, there is a risk of finding glitches in FLO).

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17.3.3 Miscellaneous Register 1

Name	reg_miscel1
Address	h06
Type	Restricted static
Default	hD05A

Default Value	Bitfield name	Description
1101 0000 ---- ----	*max_offset[7:0]*	ADC max offset Maximum offset that can be applied to the ADC column (analogically). See Section 6. and Section 19.4. Min = 0 **Default ➔ hD0 : Offset max 208 LSB** Max = hFF
---- ---- 0101 1010	*range_coeff[7:0]*	10 to 8 bit knee point Defines the knee point for the 10 to 8 bit compression. Min = h00 ➔ function with only 1 slope G=1 **Default = h5A ➔function with 3 slopes G=1/2 G=1 and G=4** Max = h92 ➔ function with only 2 slopes G=4 and G= 1/2 Note: This register is used only if range_en (@ h0A) = 1

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17.3.4 Miscellaneous Register 2

Name	reg_miscel2
Address	h07
Type	Restricted static
Default	h0A01

Default Value	Bitfield name	Description
X--- ---- ---- ----	*reserved*	
-0-- ---- ---- ----	*sync_flo_inv*	FLO signal polarity **0 ➔ FLO is not inverted (active high: FLO = 1 means that light may be turned on)** 1 ➔ FLO is inverted (active low)
--0- ---- ---- ----	*sync_len_inv*	LEN signal polarity **0 ➔ LEN is not inverted (active low: LEN = 0 means that pixels are being output)** 1 ➔ LEN is inverted (active high)
---0 ---- ---- ----	*sync_fen_inv*	FEN signal polarity 0 ➔ FEN is not inverted (active low: FEN = 0 means that pixels are being output) 1 ➔ FEN is inverted (active high)
---- 1--- ---- ----	*mask_idle_data*	Mask idle data 0 ➔D0..D9 output data may change, whatever LEN value **1 ➔ if LEN is at inactive level then D0..D9 are set to 0**
---- -0-- ---- ----	*color_en*	Color mode selection **0 ➔ B&W mode** 1 ➔Color mode (with Bayer pattern) This bit is used for defect correction, binning algorithms and for ROI size calculation. It must be set to 1 when using a color sensor.
---- --1- ---- ----	*clamp_auto_en*	Auto clamp mode 0 ➔Black level adjustment has to be done manually **1 ➔Enables automatic black level adjustment**
---- ---0 ---- ----	*roi_expanded*	ROI expanded mode **0 ➔ Programmed ROI has its origin (0,0) in the first illuminated pixel of the physical matrix** 1➔ Programmed ROI has its origin (0,0) in the first pixel of the physical matrix, including dark pixels (the 19 first black lines can be read at the beginning of the frame) Note: If roi_expanded= 1, clamp_auto_en (bit 9) must be set at 0.

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Default Value	Bitfield name	Description
---- ---- 0--- ----	*roi_flip_h*	Horizontal flip enable **0 ➔ No horizontal flip** 1 ➔ Horizontal flip
---- ---- -0-- ----	*roi_flip_v*	Vertical flip enable **0 ➔ No vertical flip** 1 ➔ Vertical flip
---- ---- --00 ----	*pattern_type[1:0]*	Test pattern type selection **00 ➔ Video output** 01 ➔ Diagonal grey scale pattern, moving (+1) on each image 10 ➔ Diagonal grey scale pattern, still image with first pixel = 0 11 ➔ Ramping pattern, with continuously incrementing pixel values
---- ---- ---- 0001	*vlr_ph_ctrl[3:0]*	Logarithmic wide dynamic range control h0 ➔ NOT allowed **h1➔ linear response** h2 **..** hF ➔ controls the knee point between linear response and log response.

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17.3.5 Clock Configuration

Name	reg_clk_cfg
Address	h08
Type	Restricted static
Default	hDB21

Default Value	Bitfield name	Description
1--- ---- ---- ----	*clk_chain_low_pwr*	CLK_CHAIN low power mode 0 ➔ CLK_CHAIN active during whole acquisition (integration and readout) **1 ➔ CLK_CHAIN active only for data readout**
-1-- ---- ---- ----	*clkout_inv*	Clock output polarity 0 ➔ DATA_CLK rising edge is simultaneous with output data change **1 ➔ DATA_CLK falling edge is simultaneous with output data change**
--0- ---- ---- ----	*freq_half*	Oscillator frequency divider **0 ➔ Oscillator frequency not divided** 1 ➔ Oscillator frequency is divided by 2 Note: If freq_half=1, the fb_calib_count_osc (@ h3C) counts the divided CLK_OSC period.
---1 ---- ---- ----	*clk_adc_on_ctrl_domain*	CLK_CTRL clock source selection Selects the clock source for CLK_CTRL (before division): 0 ➔ CLK_CHAIN **1 ➔ CLK_ADC**
---- 10-- ---- ----	*clk_on_adc_domain[1:0]*	CLK_ADC clock source selection Selects the clock source for CLK_ADC: 00 ➔ Clock from CLK_FIX pad 01 ➔ Clock from CLK_REF pad **10 ➔ Clock from internal oscillator** 11 ➔ Clock from PLL

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Default Value	Bitfield name	Description
---- --11 ---- ----	*clk_on_chain_domain [1:0]*	CLK_CHAIN clock source selection Selects the clock source for CLK_CHAIN: 00 ➔ Clock from CLK_FIX pad 01 ➔ Clock from CLK_REF pad 10 ➔ Clock from internal oscillator **11 ➔ Clock from PLL**
---- ---- 0010 ----	*div_clk_ctrl[3:0]*	CLK_CTRL frequency divider Defines the clock division ratio applied to CLK_CTRL. Min = h0 or h1 ➔ CLK_CTRL divided by DIV_CTRL = 1 **Default h2 ➔ CLK_CTRL divided by DIV_CTRL = 2** Max hF ➔ CLK_CTRL divided by DIV_CTRL = 15
---- ---- ---- 0001	*div_clk_chain[3:0]*	CLK_CHAIN frequency divider Defines the clock division ratio applied to CLK_CHAIN. Min = h0 or h1 ➔ CLK_CHAIN divided by DIV_CHAIN = 1 **Default h1 ➔ CLK_CHAIN divided by DIV_CHAIN = 1** Max hF ➔ CLK_CHAIN divided by DIV_CHAIN = 15

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17.3.6 PLL Configuration

Name	reg_pll_cfg
Address	h09
Type	Restricted static
Default	h6125

Default Value	Bitfield name	Description
-11- ---- ---- ----	*pll_od[1:0]*	PLL P parameter 00 ➔ P= 1 01 ➔ P= 2 10 ➔ Forbidden value **11 ➔ P= 4**
---0 0001 ---- ----	*pll_n[4:0]*	PLL N parameter N = 2 x (pll_n + 1) Min ➔ h00 : N = d2 **Default ➔ h01 : N = d4** Max ➔ h09 : N = d20
---- ---- 0010 0101	*pll_fb[7:0]*	PLL M parameter M = 2 x (pll_fb + 1) Min ➔ h01 : M = d4 **Default ➔ h25 : M = d76** Max ➔ hFF : M = d512

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17.3.7 CHAIN Configuration

Name	reg_chain_cfg
Address	h0A
Type	Dynamic
Default	h0200

Default Value	Bitfield name	Description
00-- ---- ---- ----	*t_int_clk_mult_factor[1:0]*	Integration time multiplication factor Multiplication factor of the fractional part of integration time. **00 ➔ x 8** 01 ➔ x 16 10 ➔ x 32 11 ➔ x 64 Note: This parameter influences each roi<i>_t_int_clk (@h0F / @h1C …)
--00 ---- ---- ----	*roi_max_id[1:0]*	Number of ROIs Defines the maximum number of ROIs to read in MIMR mode. **00 ➔ 1 ROI : ROI1** 01 ➔ 2 ROIs : ROI1 & ROI2 10 ➔ 3 ROIs : ROI1, ROI2 & ROI3 11 ➔ 4 ROIs : ROI1, ROI2, ROI3 & ROI4
---- 00-- ---- ----	*hist_bin_nb[1:0]*	Number of histogram bins Defines the maximum number of histogram bins: **00 ➔ 64 / 1 = 64 bins** 01 ➔ 64 / 2 = 32 bins 10 ➔ 64 / 4 = 16 bins 11 ➔ 64 / 8 = 8 bins (Warning, possible overflow) Note: Used only if roi_histo_en ON, in the same register
---- --10 ---- ----	*binning_div_factor[1:0]*	Binning division factor Division factor of 4-pixel sum in binning mode 00 ➔ 4-pixel sum divided by 1 01 ➔ 4-pixel sum divided by 2 **10 ➔ 4-pixel sum divided by 4** Note: Used only if roi<i>_binning_en is ON, in the same register

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Default Value	Bitfield name	Description
---- ---- 0--- ----	*roi_context_out_en*	Context output enable Enables context (header and footer) on output data **0 ➔ No context available on output** 1 ➔ Enables context on output See Note 1.
---- ---- -0-- ----	*roi_histo_en*	Histogram calculation enable Enables histogram calculation on data stream **0 ➔ No histogram calculation requested** 1 ➔ Enables histogram calculation See Note 1.
---- ---- --0- ----	*roi_ddc_en*	Defect correction enable Enables defect correction on data stream **0 ➔ No defect correction requested** 1 ➔ Enables defect correction
---- ---- ---0 ----	*range_en*	Range compression enable Enables range compression on data stream **0 ➔ No range compression requested** 1 ➔ Enables range compression Note: See range_coef (@ h06) to control range compression
---- ---- ---- 0---	*roi4_binning_en*	ROI4 binning **0 ➔ No binning requested on ROI4** 1 ➔ Enables binning on ROI4 See Note 1.
---- ---- ---- -0--	*roi3_binning_en*	ROI3 binning **0 ➔ No binning requested on ROI3** 1➔ Enables binning on ROI3 See Note 1.
---- ---- ---- --0-	*roi2_binning_en*	RIO2 binning **0 ➔ No binning requested on ROI2** 1 ➔ Enables binning on ROI2 See Note 1.
---- ---- ---- ---0	*roi1_binning_en*	ROI1 binning **0 ➔ No binning requested on ROI1** 1 ➔ Enables binning on ROI1 See Note 1.

Note 1: This parameter influences extra_line_nb (@ h04).

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17.3.8 CTRL Configuration

Name	reg_ctrl_cfg
Address	h0B
Type	Mixed: Static (s) and Restricted Static (rs)
Default	h0005

Default Value	Bitfield name	Description
--0- ---- ---- ----	*rs dum_stdby_en*	Reserved, must be kept at 0
---0 ---- ---- ----	*rs dum_pwrup_en*	Reserved, must be kept at 0
---- 0--- ---- ----	*rs dum_img_out_en*	Reserved, must be kept at 0
---- -0-- ---- ----	*s lock_dyn_reg*	Lock dynamic registers **0 ➔ Dynamic registers are not locked. Changes to dynamic registers are applied at the end of current frame** 1 ➔ Dynamic registers are locked. All changes are memorized but are not taken into account. They are applied only when lock_dyn_reg is set to 0, at the end of the current frame. Note: Depending on overlap_en (on same register), there might be a delay of 1 frame to apply changes to dynamic registers.
---- --0- ---- ----	*s trig_pad_inv*	TRIG pin polarity **0 ➔ TRIG pin is active high** 1 ➔ TRIG pin is active low
---- ---0 ---- ----	*s trig_pad_sel*	TRIG pin enable **0 ➔ TRIG pin is disabled.** 1 ➔ TRIG pin is enabled
---- ---- 00-- ----	*rs roi_flash_mode[7:6]*	ROI Flash Strobe mode selection **00 ➔ Flash Strobe OFF: FLO = 0** 01 ➔ Flash Strobe ON: FLO = 1 during integration time 10 ➔ Flash Strobe ON: FLO = 1 during integration time + readout 11 ➔ Flash Strobe ON: FLO = 1 during acquisition sequence
---- ---- --00 ----	*rs roi_readout_mode[5:4]*	ROI readout mode selection **00 ➔ 5T Global Shutter** 01 ➔ 4T + Global Reset 10 ➔ 4T + ERS 11 ➔ Reserved

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Default Value	Bitfield name	Description
---- ---- ---- 0---	*rs roi_video_en*	Video mode enable **0 ➔ Video mode disabled** 1 ➔ Acquisitions are done in video mode, with a constant frame period. See t_frame_period (@ h0C).
---- ---- ---- -1--	*rs roi_overlap_en*	Overlap mode enable 0 ➔ No overlap mode enabled **1 ➔ Acquisitions are done in overlap mode**, not used if readout_mode = 4T+GR
---- ---- ---- --0-	*s trig_rqst*	SPI trigger enable **0 ➔ SPI trigger inactive.** 1 ➔ SPI trigger calls for an acquisition
---- ---- ---- ---1	*s stdby_rqst*	STANDBY request 0 ➔ The chip is exiting STANDBY state **1 ➔ The device will re-enter STANDBY state after the end of the frame that has started to integrate.** Note: This means that, if overlap_en = 1, then STANDBY state is entered only after the end of next frame.

Caution: This register is not a simple static (s) register; it contains some restricted static (rs) bitfields. Take care not to change any 'rs' bitfields (ex: overlap_en), while changing an 's' bitfield (ex: ***trig_rqst***), when the device is not in IDLE or STANDBY state.

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17.3.9 Frame Period

Name	reg_t_frame_period
Address	h0C
Type	Dynamic
Default	h0000

Default Value	Bitfield name	Description
0000 0000 0000 0000	*t_frame_period[15:0]*	Frame period length Defines the frame period in number of lines This frame period is used in video mode if video mode is enabled. See roi_video_en (@ h0B) **Min = h0000** ➔ not taken into account Max = hFFFE ➔ Frame period of 65534 lines = 1s if CLK_CTRL @57 MHz and line_length = h70

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17.3.10 Wait Time

Name	reg_t_wait
Address	h0D
Type	Dynamic
Default	h0000

Default Value	Bitfield name	Description
0000 0000 0000 0000	*t_wait[15:0]*	ROI wait time Defines the wait time after the end of each read image, programmed in numbers of lines. **MIN = h0000 ➔ wait time = 0 line** MAX = hFFF0 ➔ d65520 lines = 1s if CLK_CTRL @57 MHz and line_length = h70 Note: 1. At the end of each ROI<i> cycle, this wait time is added with a specific roi<i>_t_wait_ext (@h10 /@h1D /…) 2. Check error_time_overflow (@ h3E) to see if roi_t_wait is too long. See frame period calculation in Section 19.2.2 for details.

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17.3.11 ROI 1 Control

This group of registers defines all the ROI1 parameters

Group Name	reg_roi1*
Group Address	h0E to h1A
Type	Dynamic

Address (Hex)	Default Value (Hex)		Bitfield name	Description
h0E	h0200		*roi1_t_int_ll[15:0]*	Integer part of ROI1 integration time Defines the integer part of the integration time in number of lines. Min = h0 ➔ Integer part of integration time is null. **Default = h200 ➔ d512 lines = 8 ms** with CLK_CTRL @57 MHz and line_length = h70 Max = hFFFE ➔ d65534 lines = 1s Note: 1. This integration time is added to the fractional part roi1_t_int_clk (@ h0F) 2. Check error_time_overflow (@ h3E) to see if this parameter is too big. See frame period calculation in Section 19.2.2 for details.
h0F	h00	--	*roi1_rep_nb[7:0]*	Number of ROI1 cycle repetitions Defines the number of ROI1 cycles that are read out = roi1_rep_nb +1 **Min h00 ➔ 1 ROI1 is read out.** Max hFF ➔ 256 ROI1 are read out.
	--	h00	*roi1_t_int_clk[7:0]*	Fractional part of ROI1 integration time Defines the fractional part of the integration time in CLK_CTRL cycles x t_int_clk_mult_factor (@ h0A) **Min= h00 ➔ fractional part of integration time is null** Max= it is recommended to take line_length_factor as a maximum. Note: If overlap_en (@ h0B) = 1, then take care to check both error_t_tint_big and error_t_tint_small (@ h3E).

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Address (Hex)	Default Value (Hex)		Bitfield name	Description
h10	h0000		*roi1_t_wait_ext[10:0]*	ROI1 extended wait time Defines an additional wait time after the end of the ROI1 cycle (last repetition of ROI1), to be added to t_wait, in number of lines **Min= h000 ➔ 0 line added** Max= h7FF ➔ d2047 lines added on twait (~32 ms if CLK_CTRL @57 MHz and line_length = h70)
h11	h00	--	*roi1_ana_gain[2:0]*	Analog gain applied on ROI1 **h0 ➔ x1** h1 ➔ x1.5 h2 ➔ x2 h3 ➔ x3 h4 ➔ x4 h5 ➔ x6 h6 ➔ x8 h7 ➔ x8
	--	h00	*roi1_dig_gain[7:0]*	Global digital gain applied on ROI1 **Min= h00 ➔ x1** Max= hFF ➔ x15.875
h12	h0006		*roi1_0l_1[10:0]*	1st line of 1st SIMR horizontal band Min = 0 **Default = h06** Max: [roi1_0l_1 + roi1_h_1] < d1036
h13	h0400		*roi1_h_1[10:0]*	Height of 1st SIMR horizontal band Min = 1 **Default = h400 ➔ d1024** Max: [roi1_0l_1 + roi1_h_1] < d1036
h14	h0006		*roi1_0c_1[10:0]*	1st column of 1st SIMR vertical band Min = 0 **Default = h006** Max: [roi1_0c_1 + roi1_w_1] < d1292
h15	h0500		*roi1_w_1[10:0]*	Width of 1st SIMR vertical band Min = 1 **Default h0500 ➔ d1280 pixels** Max: [roi1_0c_1 + roi1_w_1] < d1292
h16	h0000		*roi1_0l_2[10:0]*	1st line of 2nd SIMR horizontal band Min: [roi1_0l_1 + roi1_h_1] < roi1_0l_2 **Default = h00** Max: [roi1_0l_2 + roi1_h_2] < d1036 Note: Used only if roi1_h_2 (@ h17) > 0
h17	h0000		*roi1_h_2[10:0]*	Height of 2nd SIMR horizontal band **Min = 0 ➔ no second horizontal band** Max : [roi1_0l_2 + roi1_h_2] < d1036

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Address (Hex)	Default Value (Hex)		Bitfield name	Description
h18	h0000		*roi1_0c_2[10:0]*	1st column of 2nd SIMR vertical band Min : [roi1_0c_1 + roi1_w_1] < roi1_0c_2 **Default = h00** Max: [roi1_0c_2 + roi1_w_2] < d1292 Note: Used only if roi1_w_2 (@ h19) > 0
h19	h0000		*roi1_w_2[10:0]*	Width of 2nd SIMR vertical band **Min 0 ➔ no second vertical band** Max: [roi1_0c_2 + roi1_w_2] < d1292
h1A	h00	--	*roi1_subs_v[7:0]*	Vertical sub-sampling on ROI1 = 8/(roi1_subs_v + 8) **Min h00 ➔ sub-sampling factor 1/1** Max hFF ➔ sub-sampling factor 1/32.875
	--	h00	*roi1_subs_h[7:0]*	Horizontal sub-sampling on ROI1 = 8/(roi1_subs_h + 8) **Min h00 ➔ sub-sampling factor 1/1** Max hFF ➔ sub-sampling factor 1/32.875

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17.3.12 ROI 2 Control

This group of registers defines all the ROI2 cycle parameters

Group Name	reg_roi2*
Group Address	h1B to h23
Type	Dynamic

Address (Hex)	Default Value (Hex)		Bitfield name	Description
h1B	h0200		*roi2_t_int_ll[15:0]*	Integer part of ROI2 integration time Defines the integer part of the integration time in number of lines. Min = h0 ➔ Integer part of integration time is null. **Default = h200 ➔ d512 lines = 8 ms** with CLK_CTRL @57 MHz and line_length = h70 Max = hFFFE ➔ d65534 lines = 1s Note: 1. This integration time is added to the fractional part roi2_t_int_clk (@ h1C) 2. Check error_time_overflow (@ h3E) to see if this parameter is too big. See frame period calculation in Section 19.2.2 for details.
h1C	h00	--	*roi2_rep_nb[7:0]*	Number of ROI2 cycle repetitions Defines the number of ROI2 cycles that are read out = roi2_rep_nb +1 **Min h00 ➔ 1 ROI2 is read out.** Max hFF ➔ 256 ROI2 are read out.
	--	h00	*roi2_t_int_clk[7:0]*	Fractional part of ROI2 integration time Defines the fractional part of the integration time in CLK_CTRL cycles x t_int_clk_mult_factor (@ h0A) **Min= h00 ➔ fractional part of integration time is null** Max= it is recommended to take line_length_factor as a maximum. Note: If overlap_en (@ h0B) = 1, then take care to check both error_t_tint_big and error_t_tint_small (@ h3E).

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Address (Hex)	Default Value (Hex)		Bitfield name	Description
h1D	h0000		*roi2_t_wait_ext[10:0]*	ROI2 extended wait time Defines an additional wait time after the end of the ROI2 cycle (last repetition of ROI2), to be added to t_wait, in number of lines **Min= h000 ➔ 0 line added** Max= h7FF ➔ d2047 lines added on twait (~ 32 ms if CLK_CTRL @57 MHz and line_length = h70)
h1E	h00	--	*roi2_ana_gain[2:0]*	Analog gain applied on ROI2 **h0 ➔ x1** h1 ➔ x1.5 h2 ➔ x2 h3 ➔ x3 h4 ➔ x4 h5 ➔ x6 h6 ➔ x8 h7 ➔ x8
	--	h00	*roi2_dig_gain[7:0]*	Global digital gain applied on ROI2 **Min= h00 ➔ x1** Max= hFF ➔ x15.875
h1F	h0006		*roi2_0l_1[10:0]*	1st line of ROI2 Min = 0 **Default = h06** Max: [roi2_0l_1 + roi2_h_1] < d1036
h20	h0400		*roi2_h_1[10:0]*	Height of ROI2 Min = 1 **Default = h400 ➔ d1024** Max: [roi2_0l_1 + roi2_h_1] < d1036
h21	h0006		*roi2_0c_1[10:0]*	1st column of ROI2 Min = 0 **Default = h006** Max: [roi2_0c_1 + roi2_w_1] < d1292
h22	h0500		*roi2_w_1[10:0]*	Width of ROI2 Min = 1 **Default h0500 ➔ d1280 pixels** Max: [roi2_0c_1 + roi2_w_1] < d1292
h23	h00	--	*roi2_subs_v[7:0]*	Vertical sub-sampling on ROI2 = 8/(roi2_subs_v + 8) **Min h00 ➔ sub-sampling factor 1/1** Max hFF ➔ sub-sampling factor 1/32.875
	--	h00	*roi2_subs_h[7:0]*	Horizontal sub-sampling on ROI2 = 8/(roi2_subs_h + 8) **Min h00 ➔ sub-sampling factor 1/1** Max hFF ➔ sub-sampling factor 1/32.875

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17.3.13 ROI 3 Control

This group of registers defines all the ROI3 cycle parameters

Group Name	reg_roi3*
Group Address	h24 to h2C
Type	Dynamic

Address (Hex)	Default Value (Hex)		Bitfield name	Description
h24	h0200		*roi3_t_int_ll[15:0]*	Integer part of ROI3 integration time Defines the integer part of the integration time in number of lines. Min = h0 ➔ Integer part of integration time is null. **Default = h200 ➔ d512 lines = 8 ms** with CLK_CTRL @57 MHz and line_length = h70 Max = hFFFE ➔ d65534 lines = 1s Note: 1. This integration time is added to the fractional part roi3_t_int_clk (@ h25) 2. Check error_time_overflow (@ h3E) to see if this parameter is too big. See frame period calculation in Section 19.2.2 for details.
h25	h00	--	*roi3_rep_nb[7:0]*	Number of ROI3 cycle repetitions Defines the number of ROI3 cycles that are read out = roi3_rep_nb +1 **Min h00 ➔ 1 ROI3 is read out.** Max hFF ➔ 256 ROI3 are read out. Note: Check roi_max_id (@ h0A) to see if this ROI cycle is run
	--	h00	*roi3_t_int_clk[7:0]*	Fractional part of ROI3 integration time Defines the fractional part of the integration time in CLK_CTRL cycles x t_int_clk_mult_factor (@ h0A) for ROI3 **Min= h00 ➔ fractional part of integration time is null** Max= it is recommended to take line_length_factor as a maximum. Note: If overlap_en (@ h0B) = 1, then take care to check both error_t_tint_big and error_t_tint_small (@ h3E).

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Address (Hex)	Default Value (Hex)		Bitfield name	Description
h26	h0000		*roi3_t_wait_ext[10:0]*	ROI3 extended wait time Defines an additional wait time after the end of the ROI3 cycle (last repetition of ROI3), to be added to t_wait, in number of lines **Min= h000 ➔ 0 line added** Max= h7FF ➔ d2047 lines added on twait (~32 ms if CLK_CTRL @57 MHz and line_length = h70)
h27	h00	--	*roi3_ana_gain[2:0]*	Analog gain applied on ROI3 **h0 ➔ x1** h1 ➔ x1.5 h2 ➔ x2 h3 ➔ x3 h4 ➔ x4 h5 ➔ x6 h6 ➔ x8 h7 ➔ x8
	--	h00	*roi3_dig_gain[7:0]*	Global digital gain applied on ROI3 **Min= h00 ➔ x1** Max= hFF ➔ x15.875
h28	h0006		*roi3_0l_1[10:0]*	1st line of ROI3 Min = 0 **Default = h06** Max: [roi3_0l_1 + roi3_h_1] < d1036
h29	h0400		*roi3_h_1[10:0]*	Height of ROI3 Min = 1 **Default = h400 ➔ d1024** Max: [roi3_0l_1 + roi3_h_1] < d1036
h2A	h0006		*roi3_0c_1[10:0]*	1st column of ROI3 Min = 0 **Default = h006** Max: [roi3_0c_1 + roi3_w_1] < d1292
h2B	h0500		*roi3_w_1[10:0]*	Width of ROI3 Min = 1 **Default h0500 ➔ d1280 pixels** Max: [roi3_0c_1 + roi3_w_1] < d1292
h2C	h00	--	*roi3_subs_v[7:0]*	Vertical sub-sampling on ROI3 = 8/(roi3_subs_v + 8) **Min h00 ➔ sub-sampling factor 1/1** Max hFF ➔ sub-sampling factor 1/32.875
	--	h00	*roi3_subs_h[7:0]*	Horizontal sub-sampling on ROI3 = 8/(roi3_subs_h + 8) **Min h00 ➔ sub-sampling factor 1/1** Max hFF ➔ sub-sampling factor 1/32.875

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17.3.14 ROI 4 Control

This group of registers defines all the ROI4 cycle parameters.

Group Name	reg_roi4*
Group Address	h2D to h35
Type	Dynamic

Address (Hex)	Default Value (Hex)		Bitfield name	Description
h2D	h0200		*roi4_t_int_ll[15:0]*	Integer part of ROI4 integration time Defines the integer part of the integration time in number of lines. Min = h0 ➔ Integer part of integration time is null. **Default = h200 ➔ d512 lines = 8 ms** with CLK_CTRL @57 MHz and line_length = h70 Max = hFFFE ➔ d65534 lines = 1s Note: 1. This integration time is added to the fractional part roi4_t_int_clk (@ h2E) 2. Check error_time_overflow (@ h3E) to see if this parameter is too big. See frame period calculation in Section 19.2.2 for details.
h2E	h00	--	*roi4_rep_nb[7:0]*	Number of ROI4 cycle repetitions Defines the number of ROI4 cycles that are read out = roi4_rep_nb +1 **Min h00 ➔ 1 ROI4 is read out.** Max hFF ➔ 256 ROI4 are read out.
	--	h00	*roi4_t_int_clk[7:0]*	Fractional part of ROI4 integration time Defines the fractional part of the integration time in CLK_CTRL cycles x t_int_clk_mult_factor (@ h0A) for ROI4 **Min= h00 ➔ fractional part of integration time is null** Max= it is recommended to take line_length / t_int_clk_mult_factor as a maximum. Note: If overlap_en (@ h0B) = 1, then take care to check both error_t_tint_big and error_t_tint_small (@ h3E).

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Address (Hex)	Default Value (Hex)		Bitfield name	Description
h2F	h0000		*roi4_t_wait_ext[10:0]*	ROI4 extended wait time Defines an additional wait time after the end of the ROI4 cycle (last repetition of ROI4), to be added to t_wait, in number of lines **Min= h000 ➔ 0 line added** Max= h7FF ➔ d2047 lines added on twait (~32 ms if CLK_CTRL @57 MHz and line_length = h70)
h30	h00	--	*roi4_ana_gain[2:0]*	Analog gain applied on ROI4 **h0 ➔ x1** h1 ➔ x1.5 h2 ➔ x2 h3 ➔ x3 h4 ➔ x4 h5 ➔ x6 h6 ➔ x8 h7 ➔ x8
	--	h00	*roi4_dig_gain[7:0]*	Global digital gain applied on ROI4 **Min= h00 ➔ x1** Max= hFF ➔ x15.875
h31	h0006		*roi4_0l_1[10:0]*	1st line of ROI4 Min = 0 **Default = h06** Max: [roi4_0l_1 + roi4_h_1] < d1036
h32	h0400		*roi4_h_1[10:0]*	Height of ROI4 Min = 1 **Default = h400 ➔ d1024** Max: [roi4_0l_1 + roi4_h_1] < d1036
h33	h0006		*roi4_0c_1[10:0]*	1st column of ROI4 Min = 0 **Default = h006** Max: [roi4_0c_1 + roi4_w_1] < d1292
h34	h0500		*roi4_w_1[10:0]*	Width of ROI4 Min = 1 **Default h0500 ➔ d1280 pixels** Max: [roi4_0c_1 + roi4_w_1] < d1292
h35	h00	--	*roi4_subs_v[7:0]*	Vertical sub-sampling on ROI4 = 8/(roi4_subs_v + 8) **Min h00 ➔ sub-sampling factor 1/1** Max hFF ➔ sub-sampling factor 1/32.875
	--	h00	*roi4_subs_h[7:0]*	Horizontal sub-sampling on ROI4 = 8/(roi4_subs_h + 8) **Min h00 ➔ sub-sampling factor 1/1** Max hFF ➔ sub-sampling factor 1/32.875

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17.3.15 Green Blue and Green Red Gain Control

Name	reg_dig_gain_gb_gr
Address	h36
Type	Dynamic
Default	h8080

Default Value	Bitfield name	Description
1000 0000 ---- ----	*gb_dig_gain[7:0]*	Green blue digital gain in color version Min = h00 ➔ x0.25 **Default = h80 ➔ x1** Max = hFF ➔ x3.97 Note: Used only if color_en (@ h07)= 1
---- ---- 1000 0000	*gr_dig_gain[7:0]*	Green red digital gain in color version Min = h00 ➔ x0.25 **Default = h80 ➔ x1** Max = hFF ➔ x3.97 Note: Used only if color_en (@ h07)= 1

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17.3.16 Blue and Red Gain Control

Name	reg_dig_gain_b_r
Address	h37
Type	Dynamic
Default	h8080

Default Value	Bitfield name	Description
1000 0000 ---- ----	*b_dig_gain[7:0]*	Blue digital gain Defines the blue digital gain in color version, and general digital gain in B&W version. Min = h00 ➔ x0.25 **Default = h80 ➔ x1** Max = hFF ➔ x3.97 Note: This parameter is be used whatever the value of color_en (@ h07)
---- ---- 1000 0000	*r_dig_gain[7:0]*	Red digital gain in color version Min = h00 ➔ x0.25 **Default = h80 ➔ 1** Max = hFF ➔ x3.97 Note: This parameter is used only if color_en (@ h07)= 1

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17.3.17 Clamp & Offset Adjustments

Name	reg_clamp_offset
Address	h38
Type	Dynamic
Default	h0080

Default Value	Bitfield name	Description
0000 0000 ---- ----	*clamp_add_offset[7:0]*	Additional clamp offset Defines a signed additional (2's-complement) offset in LSB: Min = h80 ➔ -128 hFF ➔ - 1 **Default = h00 ➔ 0** h01 ➔ 1 Max = h7F ➔ 127 Note: Used only if clamp_auto_en (@ h07)= 1
---- ---- 0000 0000	*clamp_manual_offset[7:0]*	Manual clamp offset Applied offset in LSB if clamp_auto_en (@ h07)= '0' **Min = h00 ➔ 0** Max = hFF ➔ 255

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17.3.18 Clamp Configuration

Name	reg_clamp_cfg
Address	h39
Type	Restricted static
Default	h3880

Default Value	Bitfield name	Description
-011 ---- ---- ----	*init_line_nb[2:0]*	Number of init lines Number of init lines (V0) before reading matrix Min = h0 **Default = h3 ➔ 3 init lines** Max = h7
---- 1000 ---- ----	*clamp_lock_th[3:0]*	Clamp lock mechanism threshold Defines the threshold for the lock mechanism (0 to 15 LSB) : Min = h0 **Default = h8 ➔ 8 LSB threshold** Max = hF
---- ---- 1--- ----	*clamp_lock_en*	Clamp lock mechanism enable 0 ➔Disables lock mechanism **1 ➔ Enables lock mechanism during automatic black level adjustment**
---- ---- -0-- ----	*dig_cor_en*	Digital correction enable **0 ➔ Digital correction is not allowed** 1➔Allows digital correction
---- ---- --00 0000	*v0_gain[5:0]*	Clamp digital V0 correction enable **Min = h00 ➔ Bypass V0 correction** h01 ➔ Apply a V0 ratio 1/64 Max = h3F ➔ Apply a V0 ratio 63/64

17.3.19 Oscillator Programming

Name	reg_prg_osc
Address	h3A
Type	Restricted static
Default	h80C0

Default Value	Bitfield name	Description
1000 000- ---- ----	*prg_osc_vsat_adjust[6:0]*	Adjust the ADC saturation to leave room for the clamp dark signal compensation. Min = h00 **->** nominal value - 64% **Default = h40 ➔ nominal value of Vsat ADC = 850 mV (see Rext calculation)** Max = h7F -> nominal value + 64%
---- ---0 1--- ----	*prg_osc_vsat_select[1:0]*	Reserved, must be kept at 01
---- ---- -100 0000	*prg_osc_freq_adjust[6:0]*	Allows adjustment of internal oscillator frequency at 114 MHz. Min = h00 **Default = h40 ➔ default value given by R_{EXT} for a given sensor** Max = h7F

Note: The oscillator is activated only if selected as clock source by clk_on_adc_domain or clk_on_chain_domain (@ h08, or if calibration is requested (see calib_count_ref @ h3B).

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17.3.20 Calibration Count for Oscillator Calibration

Name	reg_calib_count_ref
Address	h3B
Type	Restricted static
Default	h0000

Default Value	Bitfield name	Description
0000 0000 0000 0000	*calib_count_ref[15:0]*	Oscillator calibration reference count This register has two different uses: • It sets the number of CLK_REF clock cycles to count for oscillator calibration: Min = h0001 ➔1 clock cycle for calibration phase Max = hFFFF ➔ 65535 clock cycles. Note: 1. This parameter must not be too big, because fb_calib_count_osc (@ h3C) could overflow, depending on both frequency and ratio… 2. This is NOT the number of clock cycles of the whole calibration sequence, you have to add the wake up phase for the oscillator (see t_wakeup_osc @ h43) and a few extra cycles. • Writing into this register starts a calibration. You can check the calibration progress in calib_mbx (@ h02), and retrieve the result in fb_calib_osc_count (@ h3C)

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17.3.21 Oscillator Calibration Feedback

Name	fb_calib_osc_count
Address	h3C
Type	Feedback

Bit positions	Bitfield name	Description
XXXX XXXX XXXX XXXX	*fb_calib_count_osc[15:0]*	Oscillator calibration result The calibration result is given as the number of CLK_OSC clock cycles counted.

17.3.22 Clamp Feedback

Name	fb_clamp
Address	h3D
Type	Feedback

Bit positions	Bitfield name	Description
XXXX XXXX ---- ----	*fb_ana_offset[7:0]*	Analog offset Offset applied on ADC column in LSB (0 to 255) (no dynamic loss)
---- ---- XXXX XXXX	*fb_dig_offset[7:0]*	Digital offset Digital offset applied on pixel value after ADC conversion in LSB (0 to 255)

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17.3.23 Sensor Status Feedback

Name	fb_status
Address	h3E
Type	Feedback

Bit positions	Bitfield name	Description
0000 000X ---- ----	*flag_dig_cor*	Digital Correction flag 0➔ Offset correction is done entirely in analog 1➔ Digital correction has been performed
0000 000- XX-- ----	*fb_state_main_global[1:0]*	Main global device state 00 ➔ Device is in STANDBY 01 ➔ Device is in WAKEUP (going to IDLE) 10 ➔ Device is in IDLE (waiting for new trig) 11 ➔ Device is in ACQUISITION
0000 000- --X- ----	*error_time_overflow*	Timing configuration overflow error 0 ➔ OK 1 ➔ Computed frame period is greater than hFFFE
0000 000- ---X ----	*error_corrupted_video*	Corrupted video error An error occurred on the applied frame_period: 0 ➔ OK 1 ➔ Computed frame period is greater than configured t_frame_period (@ h0C), in video mode.
0000 000- ---- X---	*error_ll_vs_xfer*	Line length error reading pixels 0 ➔ OK 1 ➔ The programmed line_length (@ h04) is too small, and pixels are still being read into matrix at end of line

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Bit positions	Bitfield name	Description
---- ---- ---- -X--	*error_ll_vs_conv*	Line length error during conversion 0 ➔ OK 1 ➔ The programmed line_length (@ h04) is too small, and conversion is still running at end of line
---- ---- ---- --X-	*error_t_int_big*	Integration time error on next image An integration time error of max 1.5 µs occurred. 0 ➔ OK 1 ➔ An error has been detected on the fractional part of the NEXT image integration time (the biggest one if we are in high dynamic configuration)
---- ---- ---- ---X	*error_t_int_small*	Integration time error on current image An integration time error of max 1.5 µs occurred. 0 ➔ OK 1 ➔ An error has been detected on the fractional part of the CURRENT image integration time (the smallest one if we are in high dynamic configuration)

17.3.24 DATA_CLK activity

Name	DATA_CLK activity
Address	h44
Type	Restricted Static

Default value	Bitfield name	Description
--1- ---- ---- ----	*clk_out_low_pwr*	Defines DATA_CLK activity: 0 ➔ DATA_CLK always active except in STANDBY state 1 ➔ DATA_CLK is active during the whole acquisition (integration, transmission and wait)

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17.3.25 Pixtime Read Width

Name	pixtime_read_width
Address	h49
Type	Restricted Static
Default	h7B71

Default value	Bitfield name	Description
0111 1011 ---- ----	*pixtime_read_5t_width[7:0]*	Pixel timing duration in 5T mode, step is CLK_CTRL period x 2 **Default = 123 clocks = 4.31 µs @57MHz**
---- ---- 0111 0001	*pixtime_read_4t_width[7:0]*	Pixel timing duration in 4T mode, step is CLK_CTRL period x 2 **Default = 113 clocks = 3.96 µs @57MHz**

17.3.26 Chip ID

Name	**chip_id**
Address	h7F
Type	Feedback
Default	h0800

Default Value		Bitfield Name	Description
0000 1000	0000 0000	chip_id[15:0]	h0800 ➔ Ruby 661 first version

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17.4 SPI Timing

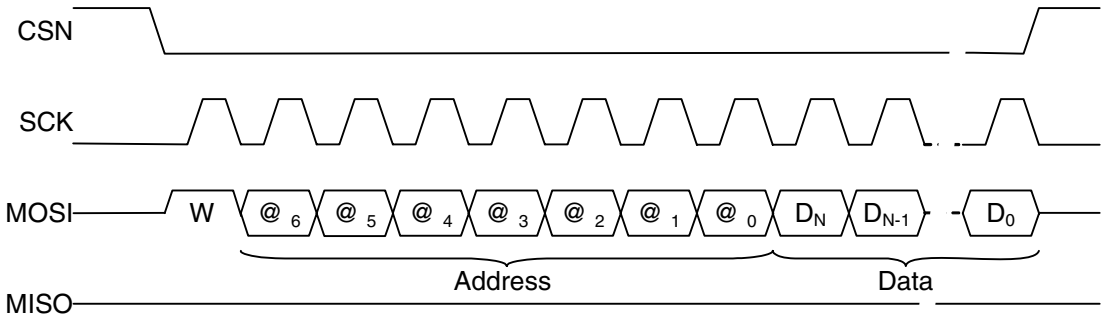
EV76C661 SPI requires CPOL = 0 and CPHA = 0.

First the SPI interface of the EV76C661 has to receive the first bit from the master on the on MOSI line which indicates if it is a read or write command. This first bit is followed by 7 bits giving the d1 to d127 addresses.

In a write sequence (see Figure 17-1: One register write sequence) first bit must be at high level. After having sent the 7 address bit - MSB first - the data are sent on the MOSI line (also MSB first).

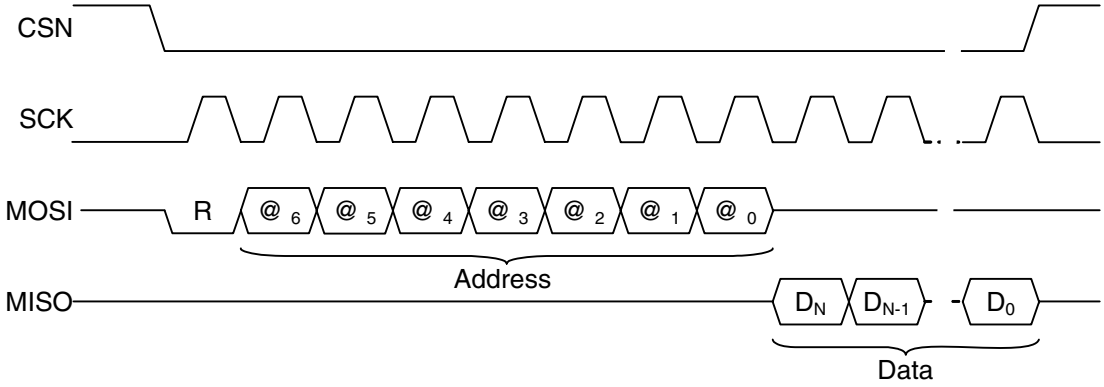
Warning : the MISO pin is not connected to a tristate pad. This means that an "OR" gate can be used on all MISO available on the SPI bus...When the CSN is inactive, the MISO is at 0.

Figure 17-1. One register write sequence



In a read sequence (see Figure 17-2: One register read sequence) first bit must be at low level. After having sent the 7 address bit MSB first, the data are read on the MISO line (also MSB first).

Figure 17-2. One register read sequence



The master can also use a burst sequence (see Figure 17-3: Burst sequence) to read or write several adjacent registers.

The end of burst sequence occurs when the CSN Chip Select line is put back into inactive state at high level.

In burst mode the internal address is automatically incremented at the end of each data read/write phase.

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For example, to read three 16-bit registers starting at address h10:

Figure 17-3. Burst sequence

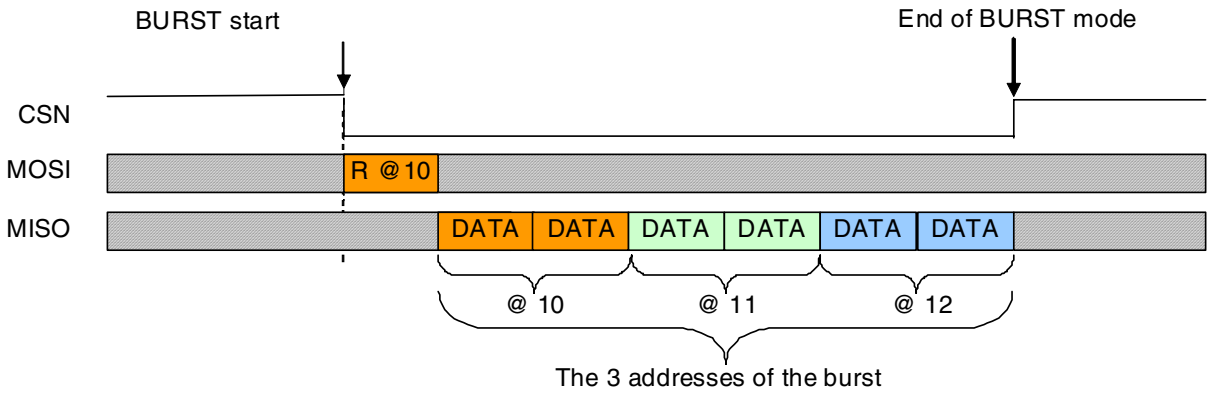
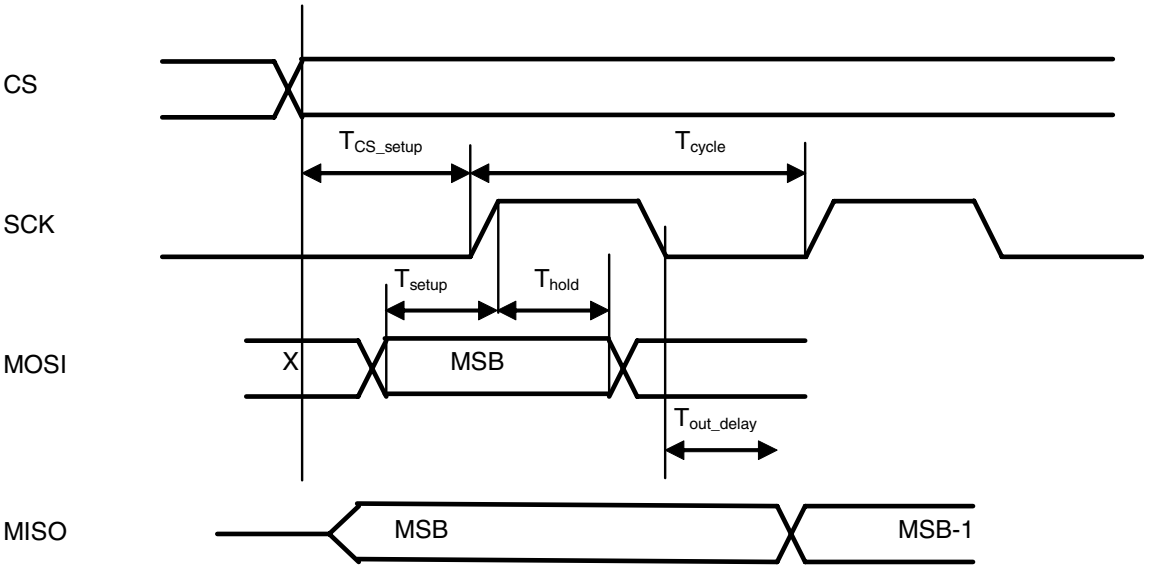


Figure 17-4. SPI timing specification



These timings depend on the process, current load, and post layout. The values given here should be considered only as general guidelines.

Table 17-3. SPI timing specification

Symbol	Typ
Tcycle	50 ns
Tsetup	<10 ns
Thold	<10 ns
Tcs_setup	>5 ns
Tout_delay	<20 ns depending on the current load

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18. Sensor States

18.1 Static States

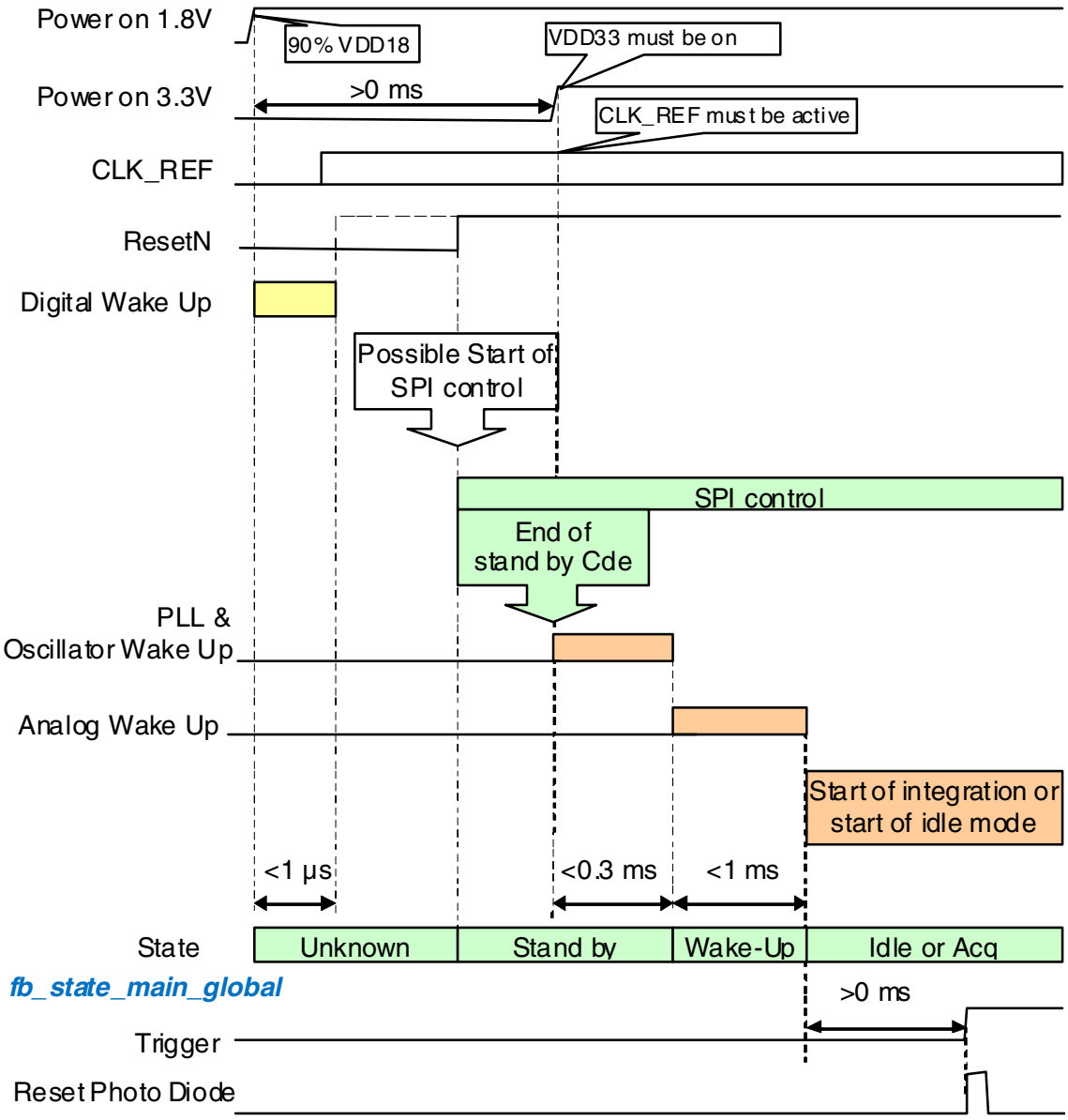
At startup, the sensor state is controlled by internal registers and by the RESETN and TRIG external signals. The registers are in a known state after a device reset. The RESETN must be pulled up and the TRIG signal can toggle.

The sensor state is indicatied in the internal status registers and from the FLO external signal.

18.1.1 Power-On Sequence

The following timing diagram shows the power up sequence initiated by a rising edge on 3.3 V and 1.8 V power supplies.

Figure 18-1. Power up sequence



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18.1.2 STANDBY

This is the lowest power consumption mode.

At power-up the sensor is in STANDBY state.

During STANDBY state the SPI registers may be read or written.

Transition from this state to IDLE state or beginning of integration has duration of less than 1 ms and is under SPI control with ***stdby_rqst*** in **<reg_ctrl_cfg>** see Section 17.3.8

18.1.3 IDLE

In IDLE state, the device is "ready to start".

During IDLE state, SPI registers can be read or written.

The sensor can start integration from this state in less than 10 µs, with an SPI command ***trig_rqst*** in **<reg_ctrl_cfg>** or with a hardware trigger on the TRIG pin if enabled by ***trig_pad_sel*** in **<reg_ctrl_cfg>** see Section 17.3.8

Transition from this state to STANDBY state is under SPI control with ***stdby_rqst*** in **<reg_ctrl_cfg>** see Section 17.3.8

18.2 Active States

Active state defines a state of the sensor during which it runs in integration or readout or is waiting for the end of an application task.

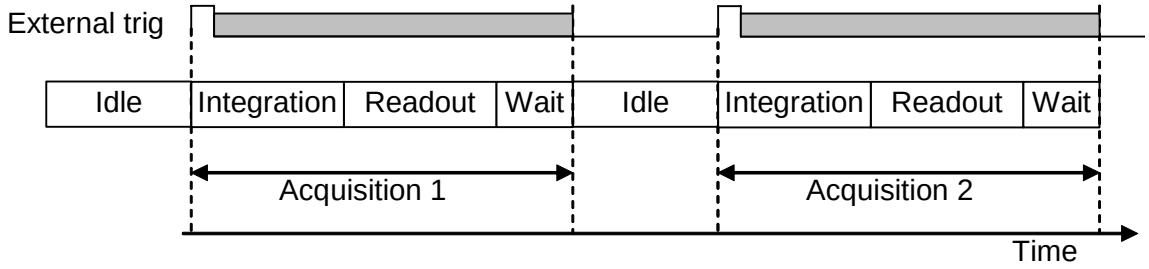
A typical acquisition sequence includes 3 states:

- Integration
- Readout
- Wait

When the sensor is waiting for a trigger it is put in IDLE state.

A short hardware or software trigger pulse starts the configured acquisition cycle. The example in Figure 18-2 is for only 1 ROI with a repetition number of 1.

Figure 18-2. Acquisition sequence example 1



The example in Figure 18-3 uses the cycle principle for 3 ROIs (***roi_max_id*** = h2) (N1, N2 and N3 are configured by the ***roi1_rep_nb***, ***roi2_rep_nb*** and ***roi3_rep_nb*** registers respectively). The Wait time (t_{WAIT}) is defined in ***<reg_t_wait>*** and is added at the end of each acquisition.

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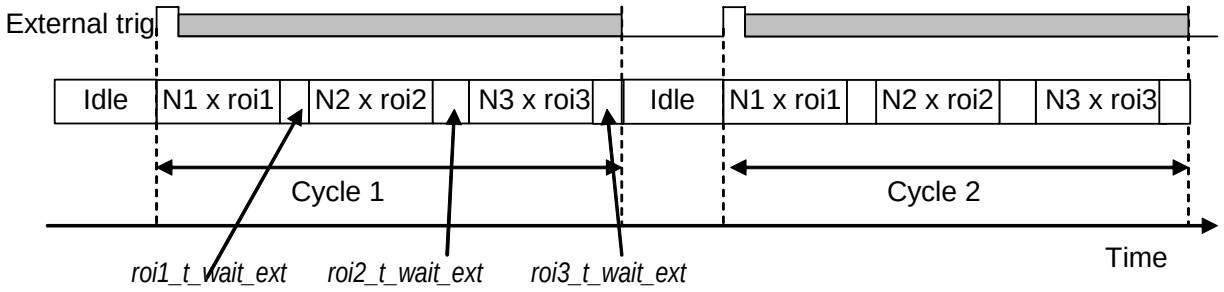
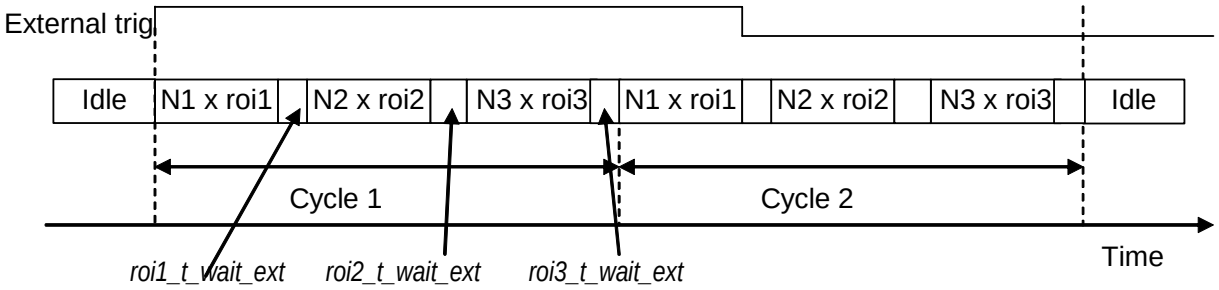
Figure 18-3. Acquisition sequence example 2



The example in Figure 18-4 shows the behavior with the trig signal kept at high level

Figure 18-4. Acquisition sequence example 3



Notes:

- The grey area indicates that any TRIG or trig_rqst pulse during this period is not taken into account.
- If the ***trig_rqst*** bit or the TRIG pin is deactivated during a cycle sequence, the sensor waits the end of the cycle before entering IDLE state.

The sensor provides three capture modes selectable by ***roi_readout_mode*** in **<reg_ctrl_cfg>** see Section 17.3.8

- Global Shutter ***roi_readout_mode*** = h0
- 4T + Global Reset ***roi_readout_mode*** = h1
- 4T + ERS ***roi_readout_mode*** = h2

With these 3 basic modes there are different possible operating sequences.

These are described in detail in the following paragraphs.

18.2.1 Global Shutter Mode

A GS acquisition sequence includes the following stages:

- Global reset of all photodiodes
- Integration simultaneously in all photodiodes
- Global transfer of all photodiode signals in sensing nodes
- Readout line by line
- Wait state

Figure 18-5. Global shutter

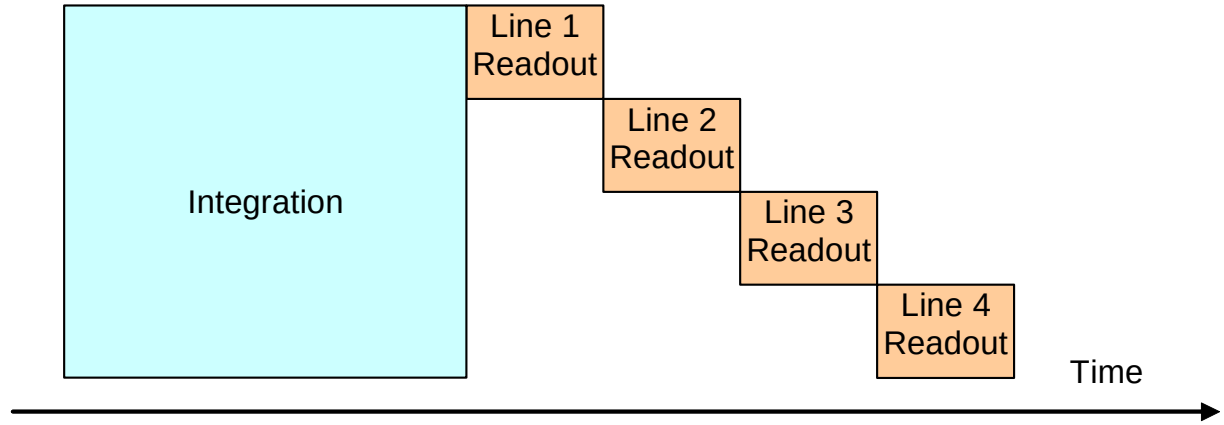
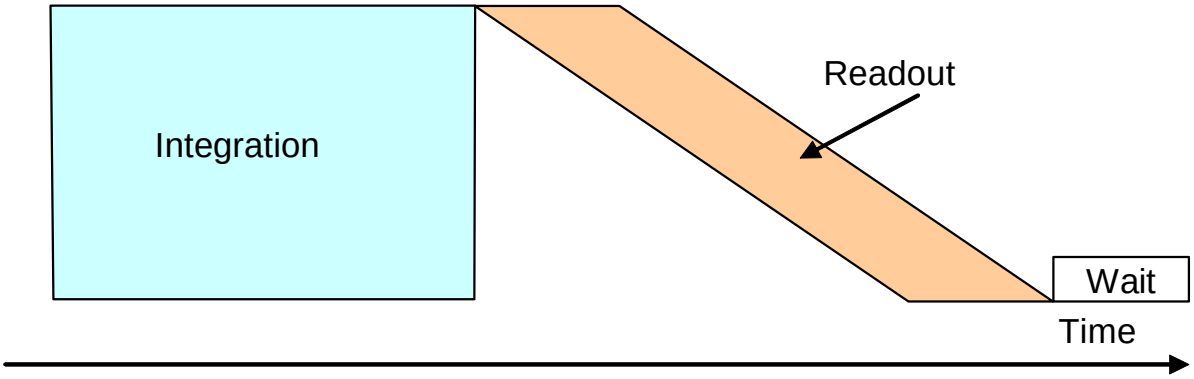


Figure 18-6. Global shutter symbolization



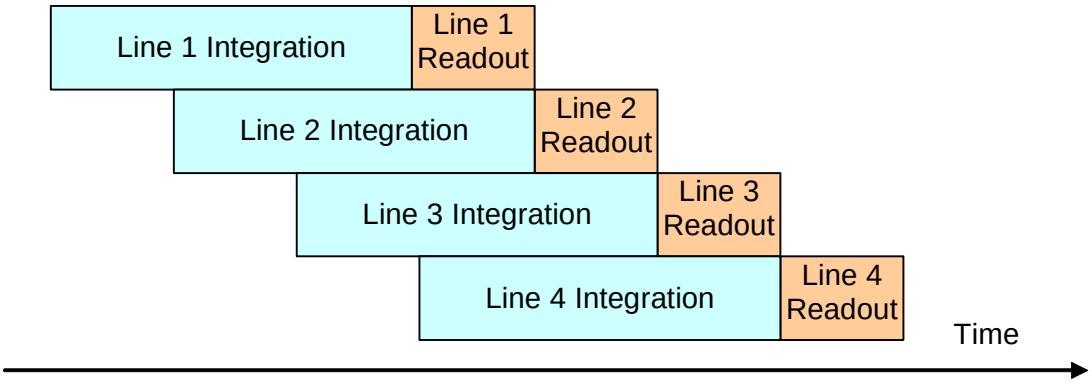
Using a 5T pixel, the global shutter mode does not allow a true CDS during pixel readout.

18.2.2 ERS Mode

Electronic Rolling Shutter (ERS) mode can perform a suppression of kTC (reset) noise. It offers better performance in terms of SNR and dynamic, but it is sensitive to the relative movement between camera and scene (called rolling shutter distortion).

In this mode every line has the same integration time duration but not at the same time. Refer to Figure 18-7.

Figure 18-7. Rolling shutter principle



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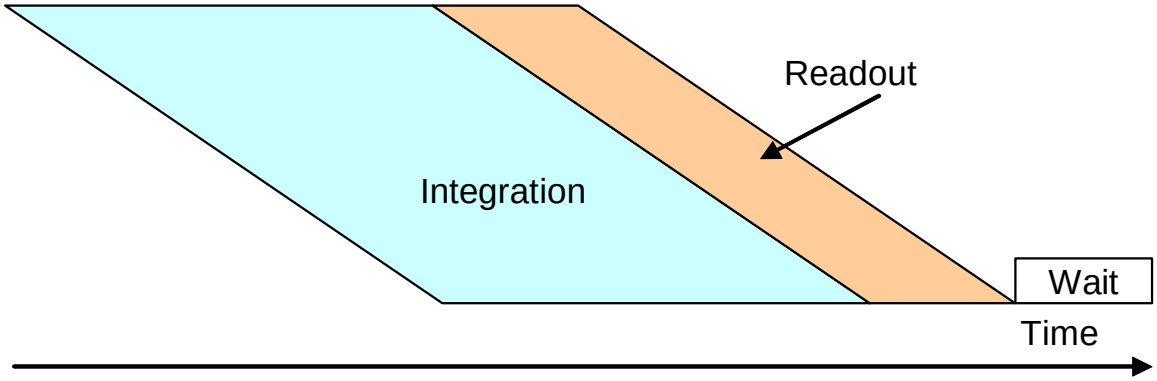
An ERS acquisition sequence includes the following states:

- Line by line integration state
- Line by line transfer and readout (this state starts at the end of the integration of the first line)
- Wait state

Figure 18-8. Rolling shutter symbolization



18.2.3 Overlap Option Definition

For ERS and GS modes, an overlap option is selectable by SPI. When it is selected the integration state of an image starts as soon as possible, before the end of the previous image.

Figure 18-9 shows ERS mode where the integration is performed line by line

Figure 18-10 shows GS mode where the integration is performed simultaneously in all photodiodes.

Twait is adjusted under SPI control.

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Figure 18-9. Overlap / Non-overlap in ERS mode

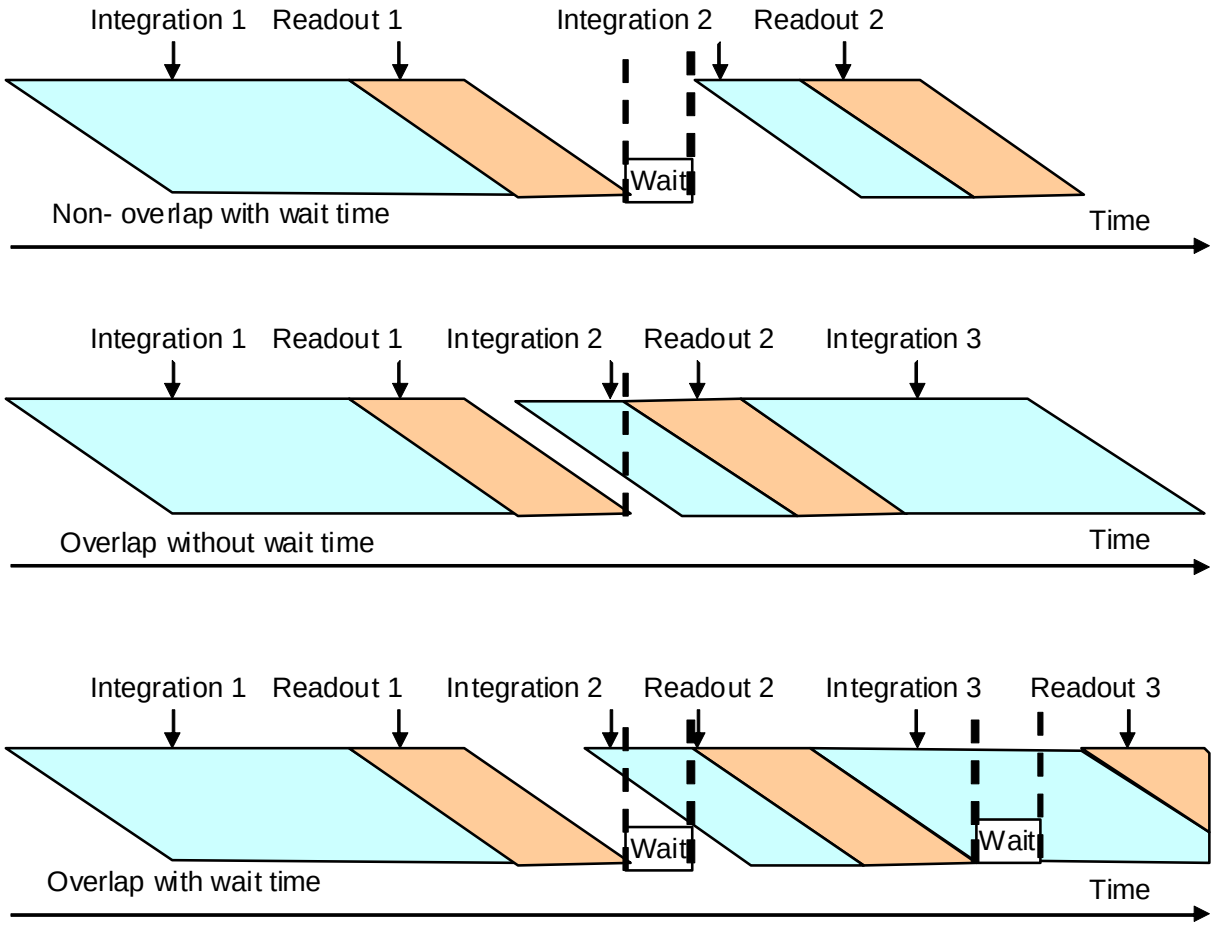

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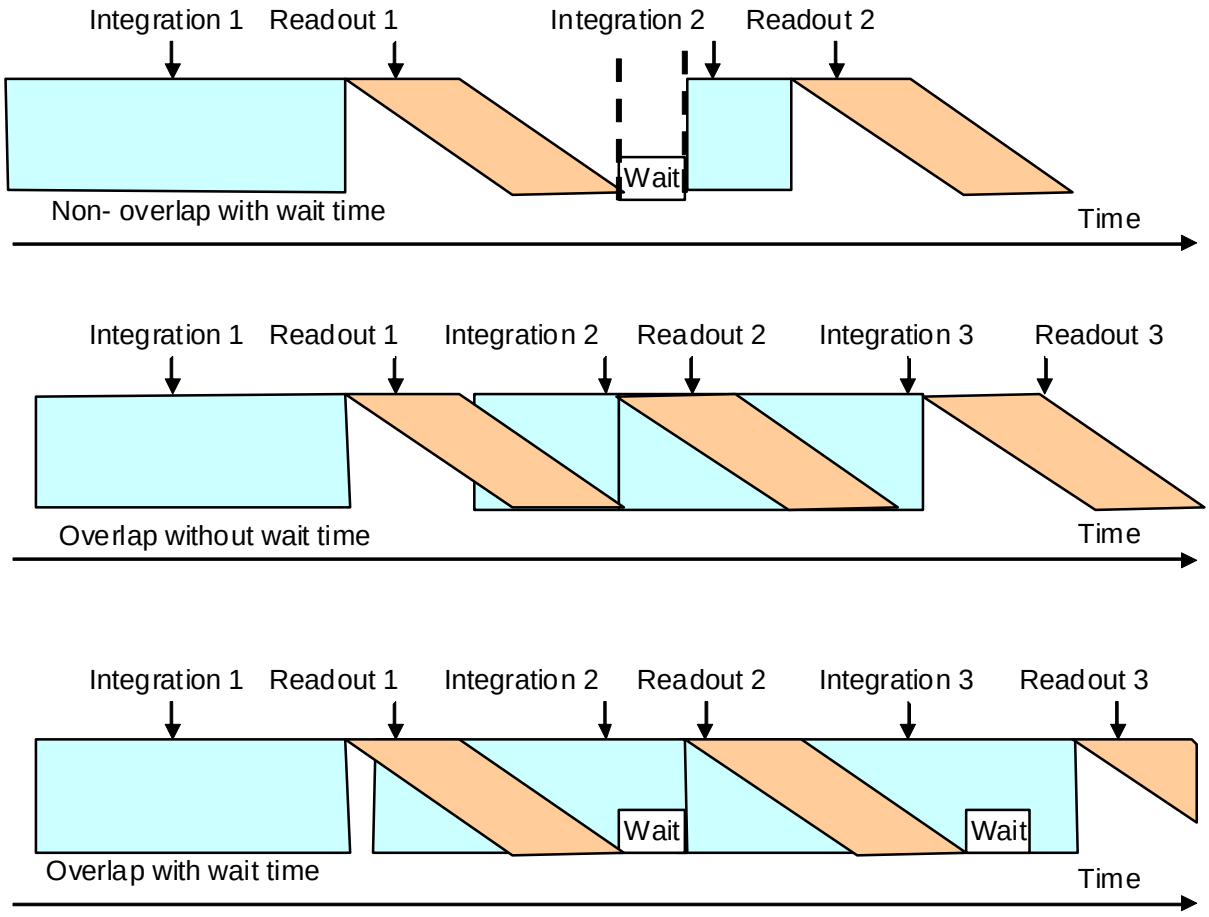
Figure 18-10. Overlap / Non-overlap in GS mode



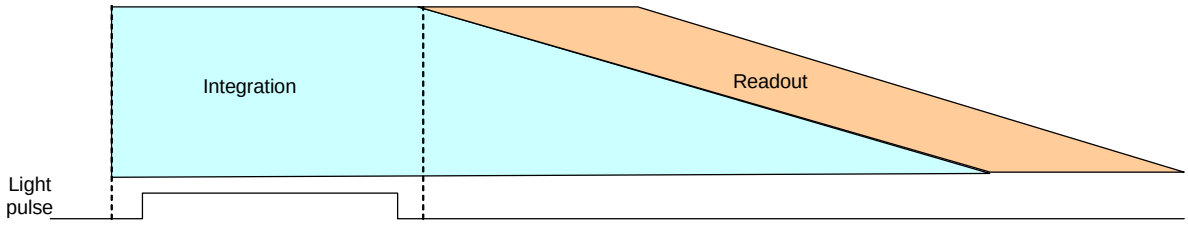
In these figures, the integration time is changed for each image to illustrate most of the different cases.

18.2.4 ERS + GR Mode

ERS + GR mode is a combination of ERS and GS modes. It allows the use of true CDS during pixel readout. It can be used for example if a synchronized light pulse is provided by the application. The moving effect may be negligible if the signal without light pulse is only negligibly different from the signal with light pulse.

The overlap option is not possible in ERS+GR mode.

Figure 18-11. ERS with Global Reset



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An ERS + GS acquisition sequence includes the following states:

- Global reset of all photodiodes and sensing nodes
- Integration stage
- Transfer, conversion and readout line by line (this state starts at the end of the integration of the first line)
- Wait stage

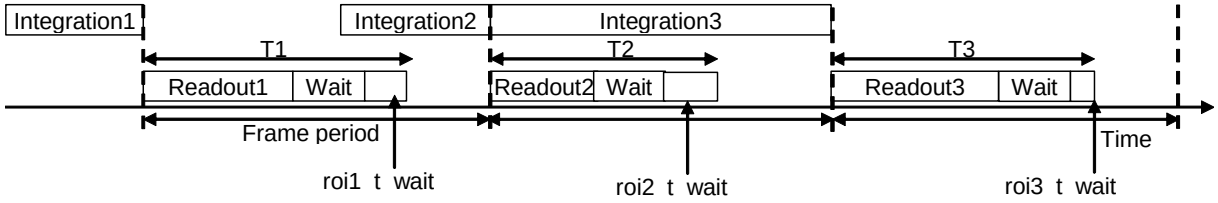
18.2.5 Video Option Definition

The Video Option can be defined for all capture modes. It is selected using the SPI. When it is selected the frame period is programmed by SPI and it constrains the integration time to a value less than the frame period.

The overlap option can be used with the video option.

Figure 18-12 gives a timing diagram showing the principle of the video option for GS readout mode with overlap option and 3 ROIs configured with only one repetition.

Figure 18-12. Video mode option



Notes:

- For each new frame, the device computes the minimum frame period value needed to correctly apply the integration time, the ROI readout and the wait time (in all frame and mode configurations). If the SPI frame period value is smaller than this minimum value, then the applied frame period is set to the computed value, and the error_corrupted_video bit is set to inform the user that the configured value is too small. The actually applied frame_period can be read in the header.

18.3 Interrupt Functions

18.3.1 Abort Function

This function allows the application to abort the current acquisition sequence. It has no effect if the sensor is in Standby or IDLE state.

The abort is taken into account:

- Immediately when the abort occurs during the integration or wait stage.
- At the end of the current line, when the abort occurs during the readout stage.

The abort sequence is cleared by writing any value in the ***flag_abort_mbx*** register.

When an abort occurs, all the register settings are preserved, so a new acquisition can be started immediately afterward. Depending on the used mode some artifacts may occur on the next image.

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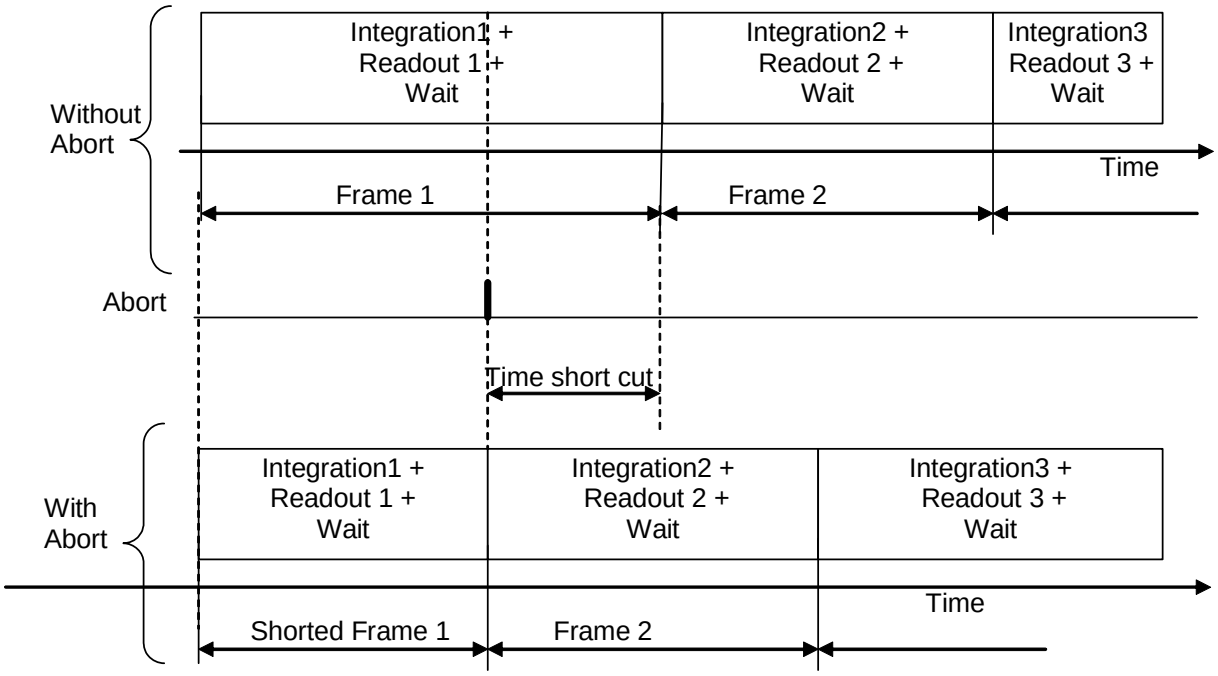
Figure 18-13. Abort timing



If an abort occurs during a MIMR sequence, then the sensor is ready to start the first integration of ROI1.

18.3.2 Reset Function

The device can be reset either by:

- Writing or reading in ***soft_reset*** see Section 17.2.2.
- Applying a low pulse on the RESETN pin (minimum pulse duration is 20 ns).

After a reset, the device returns immediately to the factory default configuration. All registers to be configured with other values must be written again.

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19. Synchronization Pulse and Timings

The FEN and LEN synchronization signals may be inverted by programming ***sync_len_inv*** and ***sync_fen_inv*** in **<reg_miscel2>**. The DATA_CLK may be inverted by using ***clk_out_inv*** in **<reg_miscel2>.** See Section 17.3.4

19.1 Clock Limits

Table 19-1. Frequency limits

Parameter	Value			
	Min	Typ	Max	Unit
CLK_REF input for PLL	5	24	50	MHz
CLK_REF input for direct use	5		120	MHz
CLK_FIX input (if used)	5		120	MHz
Duty cycle on CLK_REF and CLK_FIX	40	50	60	%
DATA-CLK , CMOS output (to be able to reach 60 fps)	85	114	120	MHz
Duty cycle on DATA-CLK		50		%

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19.2 Vertical Timings

19.2.1 Timing Diagram

Figure 19-1. Vertical timing graph

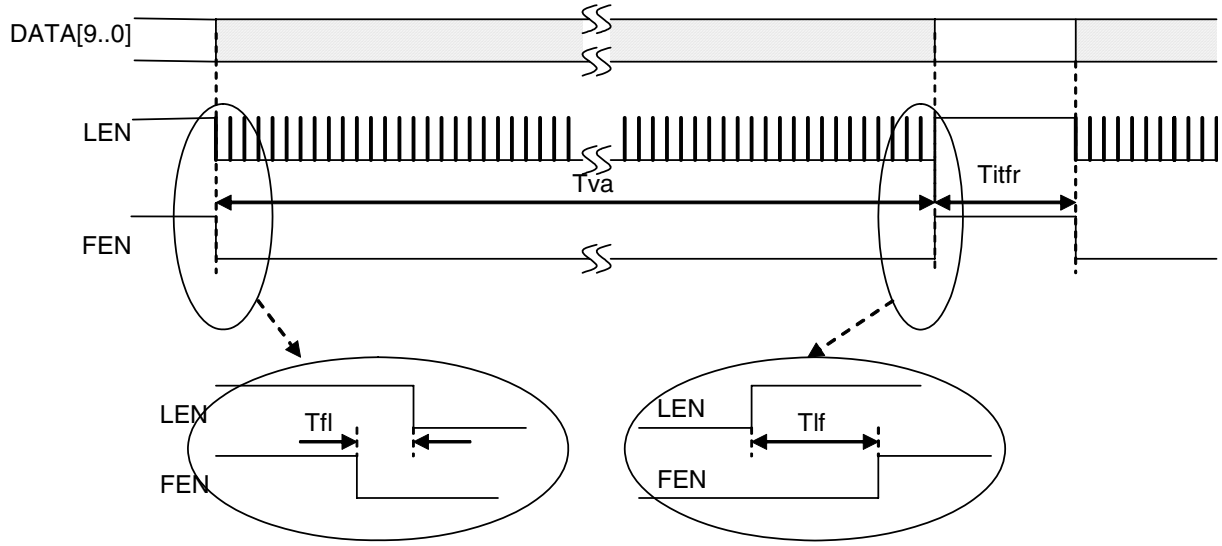

Table 19-2. Vertical timing specification

Parameter	Symbol	Nominal	Unit
Vertical valid data (1)	Tva	1024	Line period
FEN falling to LEN falling	Tfl	2 minimum	DATA_CLK
LEN rising to FEN rising	Tlf	2 minimum	DATA_CLK
Inter-frame time (2)	Titfr	Configurable	Line period

1. Depends on ROI and Sub sampling: Tva = (roi_height + 2 context_en + histo_en)
2. Titfr = t_frame_period - Tva

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19.2.2 Frame Period Calculation

The sensor runs properly in video mode if the frame period is currently programmed. The following paragraph gives the user a procedure to calculate the minimum frame period value to program (in number of lines) when ***roi_video_en***=1 (in register h0B).

If the frame period is not correct, two flags can warn the user:

- ***error_corrupt_video*** flag in the register h3E. A bad frame period will set this flag.
- ***error_corrupt_overflow*** flag in the register h3E: reg_frame_period exceeds 65534 (hFFFE) and this saturation value is applied.

Table 19-3. Registers used for frame period calculation

Entries	Register Address	Comments
reg_t_frame_period	h0C	
roiN_t_int_ll	h0E, h1B, h24, h2D	Depends on the ROI used
extra_line_nb	h04	Bits (12:15)
init_line_nb	h39	Bits (12:14)
roi_expanded	h07	Bit 8
roiN_binning_en	h0A	Bit 0,1,2 or 3
t_wait	h0D	
roiN_t_wait_ext	h10, h1D, h26, h2F	Depends on the ROI used
roi_histo_en	h0A	Bit 6
roi_context_out_en	h0A	Bit 7
roi_overlap_en	h0B	Bit 2
Roi_height		Calculated in Section 4.5.3.1

For the Frame period computation (in number of lines), the user may follow the steps above:

1. Program the minimum number of extra-lines (register ***extra_line_nb*** @ h04)
   extra_line_nb = $(2 \times roiN_binning_en + roi_histo_en + roi_context_out_en) \times 2^{roiN_binning_en}$
2. Readout time
   $Treadout = 2 + init_line_nb + (6 \times \overline{roi_expanded}) + roi_height + extra_line_nb + 1$

Minimum frame period

If ***overlap_en*** = 0 then:

$reg_t_frame_period = roiN_t_int_ll + Treadout + t_wait + roiN_t_wait_ext + t_flash_on$

If ***overlap_en*** = 1 then:

$reg_t_frame_period = MAX(roiN_t_int_ll + 1 + t_flash_on;\ Treadout + t_wait + roiN_t_wait_ext)$

The result of the frame period calculation can be read from the context data, depending on the video mode:

- If ***video_en***=1, and reg_t_frame_period ? t_frame_period_min:
  then Actual_frame_period = t_frame_period,
- If ***video_en***=0, then Actual_frame_period = t_frame_period_min

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19.2.3 Typical Frame Rate

Table 19-4 gives the possible frame rates in overlap mode with a CLK_ADC of 114 MHz.

In non-overlap mode, the integration time must be added to Tread.

Table 19-4. Frame rate example

Format	Number of columns	Number of lines	Line Length	T_{READ} (ms)	Frame Rate in ERS Mode
0.92 MP	1280	720	1792	11.2	89 fps
1.3 MP	1280	1024	1792	16.4	60.9 fps
650 kP	1280	512	1792	8.4	119.6 fps
650 kP	640	1024	1792	16.4	60.9 fps

Using sub-sampling or windowing reduces the readout time only by the reduced number of lines.

19.3 Horizontal Timings

Figure 19-2. Horizontal timing graph

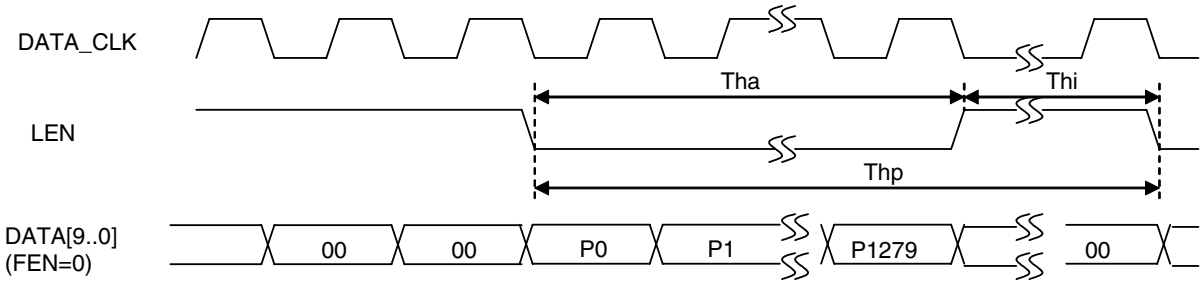

Table 19-5. Horizontal timing specification

Parameter	Symbol	Default ROI	Unit
Horizontal active pixel (1)	Tha	1280	DATA_CLK
Horizontal inactive pixel (2))	Thi	544	DATA_CLK
Horizontal period(2)	Thp	1792	DATA_CLK

1. Depends on ROI and Sub sampling.
2. Depends on line length configuration.

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19.4 Line_length Calculation

The sensor runs properly if the line length is currently programmed. The following paragraph gives the user a procedure to calculate the minimum line length value to program for correct sensor operation. Line length is calculated in number of CLK_CTRL period.

If the line length is not correct, two flags can warn the user:

- The ***error_ll_vs_conv*** flag in the register h3E. A too long conversion time will set this flag.
- The ***error_ll_vs_xfer*** flag in the register h3E. A too long data readout time will set this flag.

The user must verify both to avoid any line length programming errors.

Table 19-6. Registers used for Line Length calculation

Entries	Register Address	Comments
CLK_CTRL (MHz)	-	See Section 14.
CLK_ADC (MHz)	-	
CLK_CHAIN (MHz)	-	
Pixtime_read_5T_width	h49	Range [0;255]
Pixtime_read_4T_width	h49	Range [0;255]
Max_offset	h06	Range [0;255]
Roi_width		Calculated in Section 4.5.3

The minimum line length value to be programmed in the SPI register (@ h04) is given by the following formula in decimal:

$$line_length\ \min = \frac{\max\left[line_length_conv,\ line_length_roi\right]}{8}$$

For a 4T pixel timing:

$$line_length_conv = 4 + 2 \times pixtime_read_4T_width + \frac{(max_offset + 2^{10} + 40) \times CLK_CTRL}{CLK_ADC}$$

$$line_length_roi = \frac{ROI_width \times CLK_CTRL}{CLK_CHAIN} + \frac{40 \times CLK_CTRL}{CLK_ADC}$$

For a 5T pixel timing:

$$line_length_conv = 4 + 2 \times pixtime_read_5T_width + \frac{(max_offset + 2^{10} + 40) \times CLK_CTRL}{CLK_ADC}$$

$$line_length_roi = \frac{ROI_width \times CLK_CTRL}{CLK_CHAIN} + \frac{40 \times CLK_CTRL}{CLK_ADC}$$

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19.5 Pixel Timings

Figure 19-3. Data and sync timing diagram

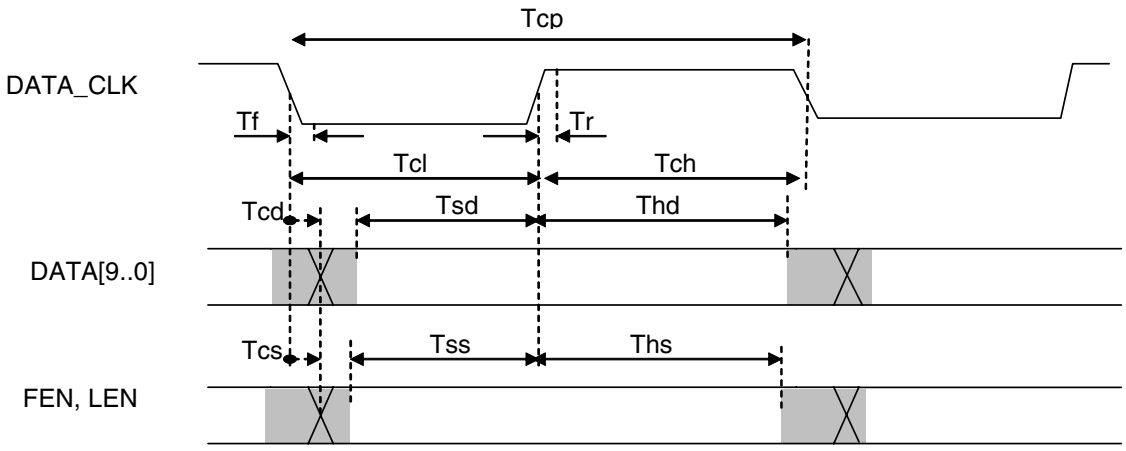


Table 19-7. Data and sync timing parameters

Parameter Definition	Symbol	Min	Typ	Max	Unit
Clock period	Tcp	8.33	8.77	200	ns
Clock low time (1)	Tcl	3.7			ns
Clock high time(1)	Tch	2			ns
DATA_CLK to data	Tcd	-0.9	-0.2	+0.7	ns
DATA_CLK to synch FEN or LEN	Tcs	-1.4	-0.6	+0.2	ns
Falling and rising edges on all signals with 10 pF load	Tr / Tf	0.8	1.5	2.6	ns

1. Including the clock input duty cycle 50 +/- 10% and frequency precision.
Setup times: Tsd = Tcl - Tcd max - Tr / Tss = Tcl - Tcs max - Tr
Hold times: Thd = Tch - Tcd min - Tr / Ths = Tch - Tcs min - Tr

19.6 FLO (Flash Strobe Output)

This signal can be used to control the light source. Several SPI registers are used to define this signal.

This signal may be inverted ***sync_flo_inv*** in **<reg_miscel2>** see Section 17.3.4 (in the timings FLO is shown non inverted)

The FLO control mode can be selected using ***roi_flash_mode*** in **<reg_ctrl_cfg>** see Section 17.3.8

- FLO signal may be stuck at 1 or at 0 ***roi_flash_mode*** = h3 or h0 respectively.
- FLO1 can be calculated based on integration time only ***roi_flash_mode*** = h1
- FLO2 can be calculated based on integration time plus readout time ***roi_flash_mode*** = h2

  The timings can be adjusted using ***t_flash_del_off*** and ***t_flash_del_on*** in **<reg_flash_delay>** see Section 17.3.2

Programming the FLO depends on the selected mode.

19.6.1 FLO in GS Mode

In this mode use only the FLO based on integration time only . (FLO1)

Figure 19-4. FLO timing, serial mode GS

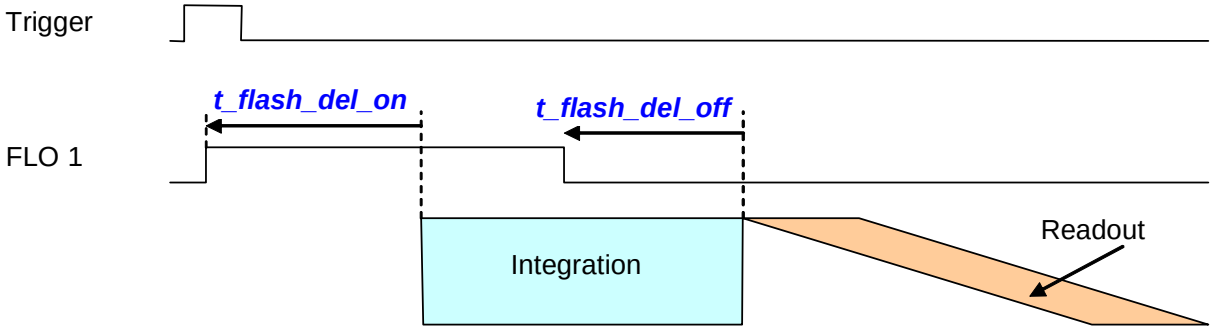
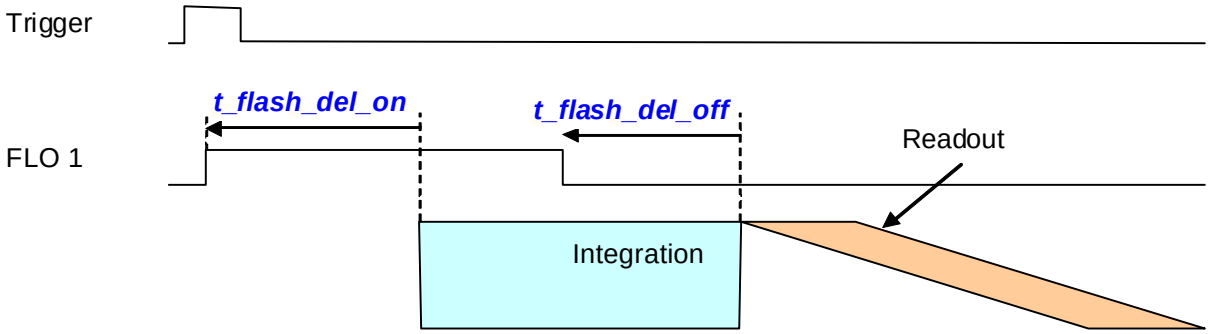


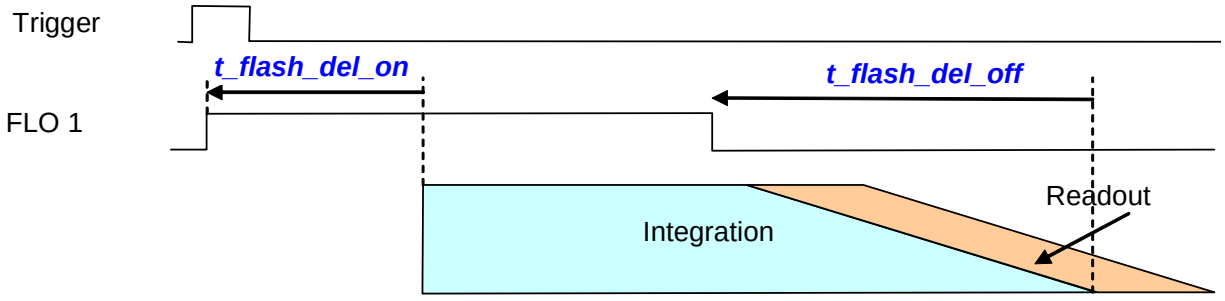
Figure 19-5. FLO timing, overlap mode GS



19.6.2 FLO in 4T + GR Mode

In this mode the FLO based on integration time only should be used. (FLO1). The Flash strobe should be switched off before readout.

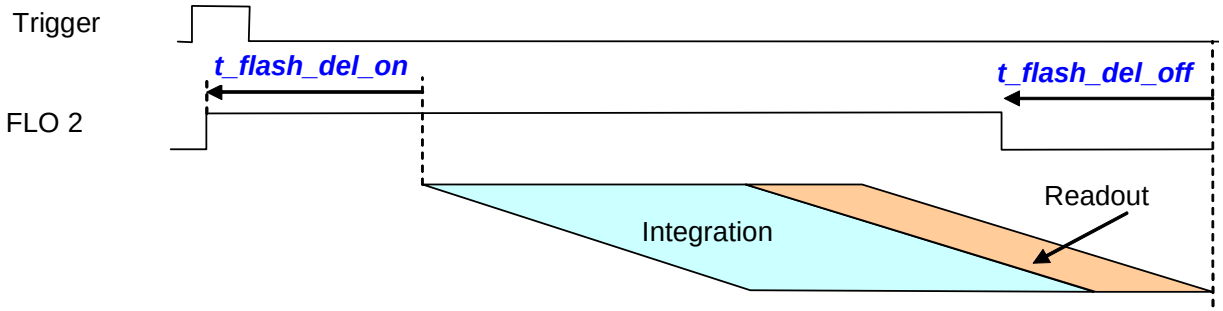
Figure 19-6. FLO timing, 4T + GR mode



19.6.3 FLO in 4T ERS Mode

In this mode the FLO based on integration time + readout should be used. (FLO2). Using ***t_flash_del_off*** at 0 allows all overlap integration conditions.

Figure 19-7. FLO timing, serial mode ERS



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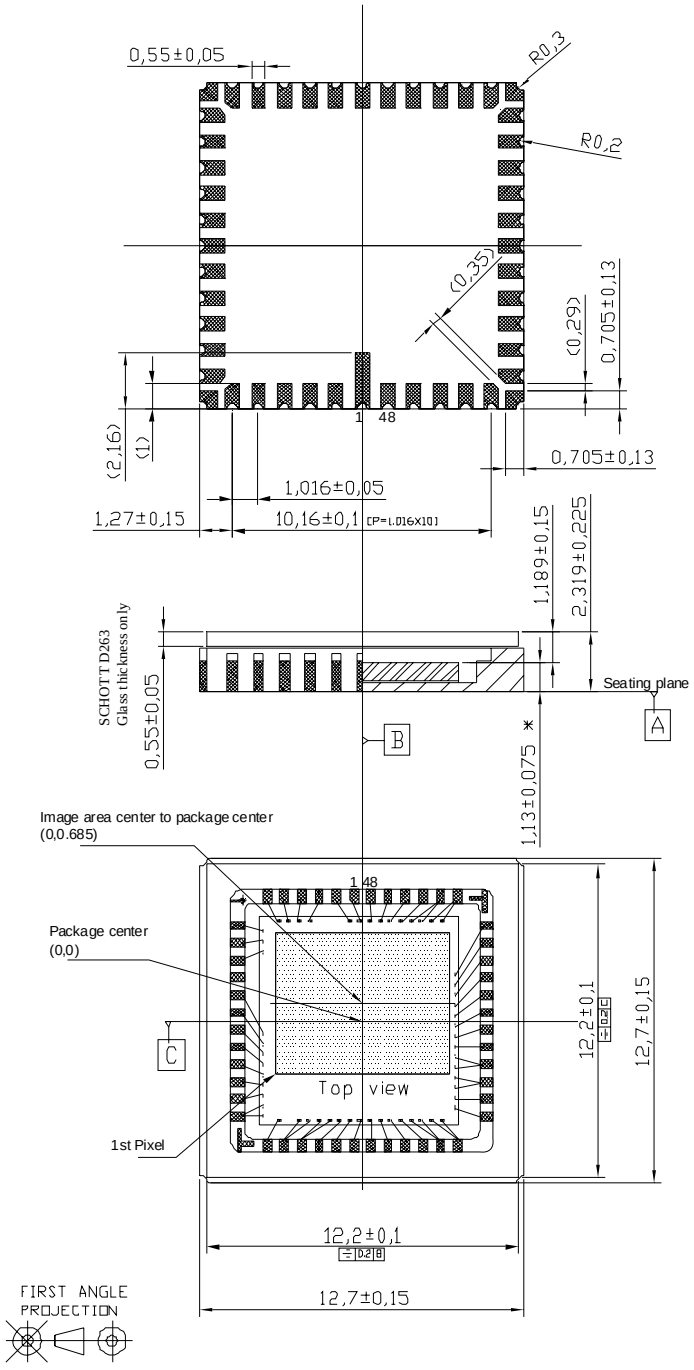
20. Package Specification

Figure 20-1. CLCC 48 package drawing



Sensor Mechanical Drawing

Maximun tilt of image area diagonal to seating plane ref A: 80µm
Maximun rotation of image area to ref B and C: 1°
Die positioning to ref B and C : +/-125µm

* Not including the tilt specification

note: Plating
Ni : 2µm Min
Au: 0.50 µm min

RoHS compliant

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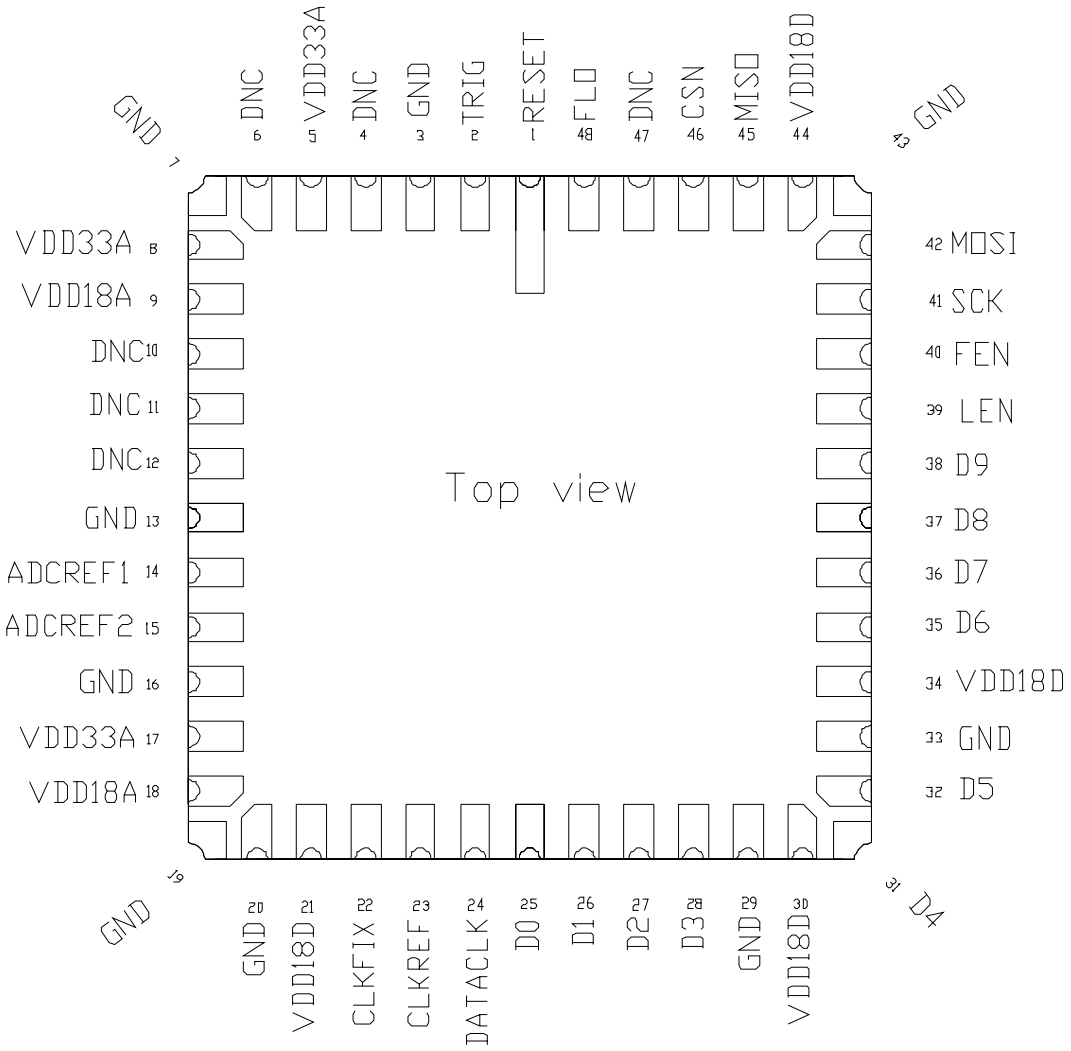
Table 20-1. Window Characteristics

Parameter	Specification
Window material	SCHOTT D263
Window thickness	0.55+/-0.03 mm
Window index	ne = 1.5255
Anti Reflective Coating	on both sides
Transmittance	>97% (400nm to 900nm)

Figure 20-2. CLCC 48 Package Pinout drawing



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21. Input/Output List

Table 21-1. I/O list

Name	Function / Description	I/O	Pin N°
VDD33A	3.3 V supply voltage for analog domain	POWER (1)	5, 8, 17
VDD18A	1.8 V Analog power, decoupling	POWER(1)	9, 18
VDD18D	1.8 V supply voltage for digital domain	POWER(1)	21, 30, 34, 44
GND	Grounds	POWER (2)	3, 7, 13, 16, 19, 20, 29, 33, 43
Test	Test pins	DNC(3)	10, 11, 12, 47
RESETN	Reset control	IN	1
TRIG	Trigger input with pull-down	IN	2
VREFP_1	VREFP supply for matrix	DNC (3)	4
VREFP_2	VREFP supply for line decoder	DNC(3)	6
ADC_REF_1	Adjusts ADC range by inserting a resistor between these two pins.	IN/OUT	14
ADC_REF_2		IN/OUT	15
CLK_FIX	Clock input fixed	IN	22
CLK_REF	Reference Clock input	IN	23
DATA_CLK	Data output clock	OUT	24
DATA 0	Data 0	OUT	25
DATA 1	Data 1	OUT	26
DATA 2	Data 2	OUT	27
DATA 3	Data 3	OUT	28
DATA 4	Data 4	OUT	31
DATA 5	Data 5	OUT	32
DATA 6	Data 6	OUT	35
DATA 7	Data 7	OUT	36
DATA 8	Data 8	OUT	37
DATA 9	Data 9	OUT	38
LEN	Line ENable	OUT	39
FEN	Frame ENable	OUT	40
SCK	SPI Clock input	IN	41
MOSI	SPI Data Input in slave mode,	IN	42
MISO	SPI Data Output in slave mode,	OUT	45
CSN	SPI Chip Select Enable	IN	46
FLO	Flash Strobe Output	OUT	48

1. All power pins with the same name must be connected to the same power supply
2. All grounds must be connected.
3. DNC stands for Do Not Connect

22. Document Conventions and Acronyms

Table 22-1. Glossary of acronyms

B&W	Black and white
CDS	Correlated double sampling
DNC	Do not connect
DSNU	Dark signal non-uniformity
EMC	Electro Magnetic Compatibility
ERS	Electronic rolling shutter
FPN	Fixed pattern noise
fps	Frames per second
GR	Global reset
GS	Global shutter
IR	Infrared
LSB	Least significant bit
MIMR	Multiple integration multiple ROI
MSB	Most significant bit
MSL	Moisture sensitivity level
PGA	Programmable gain amplifier
PRNU	Photo response non-uniformity
ROI	Region of interest
Sat	Saturation value
SIMR	Single integration multiple ROI
SPI	Serial peripheral interface
Tint	Integration time

22.1 SPI Register and Bitfield Names

SPI registers and bitfield names are shown in blue bold italics as follows:

example_reg_name for the entire register

example_bitfield_name in **< example_reg_name>** for part of the register

22.2 Numbering Conventions

Hexadecimal numbers are prefixed by “h”.

In register descriptions, decimal numbers are prefixed by “d”.

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23. Precautions for Using the Device

23.1 Absolute Maximum Ratings

Table 23-1. Absolute maximum ratings

Parameter	Value
VDD18D digital supply voltage	-0.25 V; 2.2 V
VDD18A analog supply voltage	-0.25 V; 2.2 V
VDD33A analog supply voltage	-0.25 V; 4 V
DC voltage at any input pin	-0.25 V; V_{DD18D} +0.25 V
Storage temperature	-40°C to + 85°C
Operating temperature	-30°C to + 65°C

- Stresses above those listed under Absolute Maximum Ratings might cause permanent device failure. Functioning at or above these limits is not recommended.
- Exposure to absolute maximum ratings for extended periods might affect reliability.
- All power pins with the same name must be connected to the same power supply.
- All grounds must be connected.

23.2 ESD

The EV76C661 is resistant up to 2 kV (HBM). To avoid accumulation of charges and to prevent electrical field formation, the following precautions must be taken during manipulation:

- Wear anti-static gloves or finger cots, anti-static clothes and shoes.
- Protect workstation with a conductive ground sheet.
- Use conductive boxes.

23.3 Cleaning the Window

The EV76C661 sensor is an optical device. All precautions must be taken to prevent dust or scratches on the input window. If the window needs to be cleaned, use the procedure described here.

23.3.1 Equipment

- Ethanol.
- Cleaning medium (wipes, optical paper, cotton buds).
- Filtered blow-off gun (preferably with static charge neutralizing capability).
- Area protected from electrostatic discharges and equipped with ground straps.

23.3.2 Preparations

- Wear vinyl gloves or finger cots without talcum powder.
- Make use of anti-ESD equipment: ground straps, ionizers etc.

23.3.3 Recommendations

- Never clean with a dry cleaning medium.
- Soak the cleaning medium with alcohol and do not pour it directly on the window.
- Clean the window only if necessary.

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23.3.4 Operating Procedure

- Clean the glass window with an air-jet (using the blow-off gun).
- If stains or dust remain;
  - Soak the cleaning medium with alcohol and wipe the glass window in a single movement from one side to another.
  - Always use a clean part of the cleaning medium for each new attempt.
  - Adapt the speed of the wiping action to let alcohol evaporate without leaving traces.
  - Optionally, use the blow-off gun to clean the window once more.

24. Standards Compliance

The EV76C661 sensor conforms to the following standards:

- RoHS compliant
- Product qualification according to JEDEC JESD47
- MSL 3 compliant

25. Ordering Codes

- EV76C661ABT-EQTR for monochrome product
- EV76C661ACT-EQTR for Bayer product

For other packaging or other CFA please contact e2v.

The sensors are delivered in Jedec trays.

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1. Cyclone IV Device Datasheet

附录3：《FPGA ALTERA CycloneIV 技术参数手册》

CYIV-53001-1.8

This chapter describes the electrical and switching characteristics for Cyclone® IV devices. Electrical characteristics include operating conditions and power consumption. Switching characteristics include transceiver specifications, core, and periphery performance. This chapter also describes I/O timing, including programmable I/O element (IOE) delay and programmable output buffer delay.

This chapter includes the following sections:

- "Operating Conditions" on page 1–1
- "Power Consumption" on page 1–16
- "Switching Characteristics" on page 1–16
- "I/O Timing" on page 1–37
- "Glossary" on page 1–37

Operating Conditions

When Cyclone IV devices are implemented in a system, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of Cyclone IV devices, you must consider the operating requirements described in this chapter.

Cyclone IV devices are offered in commercial, industrial, extended industrial and, automotive grades. Cyclone IV E devices offer –6 (fastest), –7, –8, –8L, and –9L speed grades for commercial devices, –8L speed grades for industrial devices, and –7 speed grade for extended industrial and automotive devices. Cyclone IV GX devices offer –6 (fastest), –7, and –8 speed grades for commercial devices and –7 speed grade for industrial devices.

For more information about the supported speed grades for respective Cyclone IV devices, refer to the *Cyclone IV FPGA Device Family Overview* chapter.

Cyclone IV E devices are offered in core voltages of 1.0 and 1.2 V. Cyclone IV E devices with a core voltage of 1.0 V have an 'L' prefix attached to the speed grade.

In this chapter, a prefix associated with the operating temperature range is attached to the speed grades; commercial with a "C" prefix, industrial with an "I" prefix, and automotive with an "A" prefix. Therefore, commercial devices are indicated as C6, C7, C8, C8L, or C9L per respective speed grade. Industrial devices are indicated as I7, I8, or I8L. Automotive devices are indicated as A7.

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Cyclone IV E industrial devices I7 are offered with extended operating temperature range.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Cyclone IV devices. The values are based on experiments conducted with the device and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied at these conditions. Table 1–1 lists the absolute maximum ratings for Cyclone IV devices.

CAUTION

Conditions beyond those listed in Table 1–1 cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time have adverse effects on the device.

Table 1–1. Absolute Maximum Ratings for Cyclone IV Devices *(1)*

Symbol	Parameter	Min	Max	Unit
V_{CCINT}	Core voltage, PCI Express® (PCIe®) hard IP block, and transceiver physical coding sublayer (PCS) power supply	–0.5	1.8	V
V_{CCA}	Phase-locked loop (PLL) analog power supply	–0.5	3.75	V
V_{CCD_PLL}	PLL digital power supply	–0.5	4.5	V
V_{CCIO}	I/O banks power supply	–0.5	3.75	V
V_{CC_CLKIN}	Differential clock input pins power supply	–0.5	4.5	V
V_{CCH_GXB}	Transceiver output buffer power supply	–0.5	3.75	V
V_{CCA_GXB}	Transceiver physical medium attachment (PMA) and auxiliary power supply	–0.5	3.75	V
V_{CCL_GXB}	Transceiver PMA and auxiliary power supply	–0.5	1.8	V
V_I	DC input voltage	–0.5	4.2	V
I_{OUT}	DC output current, per pin	–25	40	mA
T_{STG}	Storage temperature	–65	150	°C
T_J	Operating junction temperature	–40	125	°C

Note to Table 1–1:

(1) Supply voltage specifications apply to voltage readings taken at the device pins with respect to ground, not at the power supply.

Maximum Allowed Overshoot or Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 1–2 and undershoot to –2.0 V for a magnitude of currents less than 100 mA and for periods shorter than 20 ns. Table 1–2 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage over the lifetime of the device. The maximum allowed overshoot duration is specified as a percentage of high-time over the lifetime of the device.

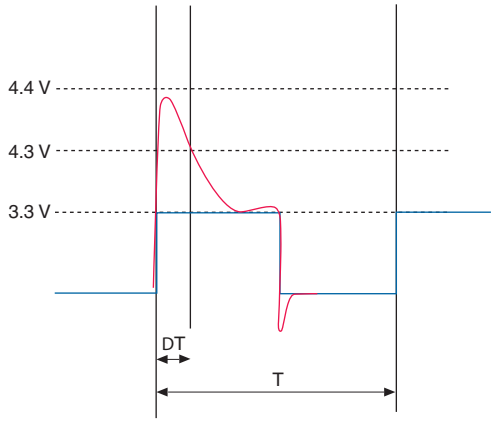
A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 4.3 V can only be at 4.3 V for 65% over the lifetime of the device; for a device lifetime of 10 years, this amounts to 65/10ths of a year.

Table 1–2. Maximum Allowed Overshoot During Transitions over a 10-Year Time Frame for Cyclone IV Devices

Symbol	Parameter	Condition (V)	Overshoot Duration as % of High Time	Unit
V_i	AC Input Voltage	V_I = 4.20	100	%
		V_I = 4.25	98	%
		V_I = 4.30	65	%
		V_I = 4.35	43	%
		V_I = 4.40	29	%
		V_I = 4.45	20	%
		V_I = 4.50	13	%
		V_I = 4.55	9	%
		V_I = 4.60	6	%

Figure 1–1 shows the methodology to determine the overshoot duration. The overshoot voltage is shown in red and is present on the input pin of the Cyclone IV device at over 4.3 V but below 4.4 V. From Table 1–2, for an overshoot of 4.3 V, the percentage of high time for the overshoot can be as high as 65% over a 10-year period. Percentage of high time is calculated as ([delta T]/T) × 100. This 10-year period assumes that the device is always turned on with 100% I/O toggle rate and 50% duty cycle signal. For lower I/O toggle rates and situations in which the device is in an idle state, lifetimes are increased.

Figure 1–1. Cyclone IV Devices Overshoot Duration



Recommended Operating Conditions

This section lists the functional operation limits for AC and DC parameters for Cyclone IV devices. Table 1–3 and Table 1–4 list the steady-state voltage and current values expected from Cyclone IV E and Cyclone IV GX devices. All supplies must be strictly monotonic without plateaus.

Table 1–3. Recommended Operating Conditions for Cyclone IV E Devices (1), (2) (Part 1 of 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCINT} (3)	Supply voltage for internal logic, 1.2-V operation	—	1.15	1.2	1.25	V
	Supply voltage for internal logic, 1.0-V operation	—	0.97	1.0	1.03	V
V_{CCIO} (3), (4)	Supply voltage for output buffers, 3.3-V operation	—	3.135	3.3	3.465	V
	Supply voltage for output buffers, 3.0-V operation	—	2.85	3	3.15	V
	Supply voltage for output buffers, 2.5-V operation	—	2.375	2.5	2.625	V
	Supply voltage for output buffers, 1.8-V operation	—	1.71	1.8	1.89	V
	Supply voltage for output buffers, 1.5-V operation	—	1.425	1.5	1.575	V
	Supply voltage for output buffers, 1.2-V operation	—	1.14	1.2	1.26	V
V_{CCA} (3)	Supply (analog) voltage for PLL regulator	—	2.375	2.5	2.625	V
V_{CCD_PLL} (3)	Supply (digital) voltage for PLL, 1.2-V operation	—	1.15	1.2	1.25	V
	Supply (digital) voltage for PLL, 1.0-V operation	—	0.97	1.0	1.03	V
V_I	Input voltage	—	–0.5	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	—	85	°C
		For industrial use	–40	—	100	°C
		For extended temperature (5)	–40	—	125	°C
		For automotive use	–40	—	125	°C
t_{RAMP}	Power supply ramp time	Standard power-on reset (POR) (6)	50 µs	—	50 ms	—
		Fast POR (7)	50 µs	—	3 ms	—

Table 1–3. Recommended Operating Conditions for Cyclone IV E Devices (1), (2) (Part 2 of 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{Diode}	Magnitude of DC current across PCI-clamp diode when enable	—	—	—	10	mA

Notes to Table 1–3:

(1) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades.

(2) V_{CCIO} for all I/O banks must be powered up during device operation. All VCCA pins must be powered to 2.5 V (even when PLLs are not used) and must be powered up and powered down at the same time.

(3) V_{CC} must rise monotonically.

(4) V_{CCIO} powers all input buffers.

(5) The I7 devices support extended operating junction temperature up to 125°C (usual range is –40°C to 100°C). When using I7 devices at the extended junction temperature ranging from –40°C to 125°C, select C8 as the target device when designing in the Quartus® II software. The I7 devices meet all C8 timing specifications when I7 devices operate beyond 100°C and up to 125°C.

(6) The POR time for Standard POR ranges between 50 and 200 ms. Each individual power supply must reach the recommended operating range within 50 ms.

(7) The POR time for Fast POR ranges between 3 and 9 ms. Each individual power supply must reach the recommended operating range within 3 ms.

Table 1–4. Recommended Operating Conditions for Cyclone IV GX Devices (Part 1 of 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCINT} (3)	Core voltage, PCIe hard IP block, and transceiver PCS power supply	—	1.16	1.2	1.24	V
V_{CCA} (1), (3)	PLL analog power supply	—	2.375	2.5	2.625	V
V_{CCD_PLL} (2)	PLL digital power supply	—	1.16	1.2	1.24	V
V_{CCIO} (3), (4)	I/O banks power supply for 3.3-V operation	—	3.135	3.3	3.465	V
	I/O banks power supply for 3.0-V operation	—	2.85	3	3.15	V
	I/O banks power supply for 2.5-V operation	—	2.375	2.5	2.625	V
	I/O banks power supply for 1.8-V operation	—	1.71	1.8	1.89	V
	I/O banks power supply for 1.5-V operation	—	1.425	1.5	1.575	V
	I/O banks power supply for 1.2-V operation	—	1.14	1.2	1.26	V
V_{CC_CLKIN} (3), (5), (6)	Differential clock input pins power supply for 3.3-V operation	—	3.135	3.3	3.465	V
	Differential clock input pins power supply for 3.0-V operation	—	2.85	3	3.15	V
	Differential clock input pins power supply for 2.5-V operation	—	2.375	2.5	2.625	V
	Differential clock input pins power supply for 1.8-V operation	—	1.71	1.8	1.89	V
	Differential clock input pins power supply for 1.5-V operation	—	1.425	1.5	1.575	V
	Differential clock input pins power supply for 1.2-V operation	—	1.14	1.2	1.26	V

Table 1–4. Recommended Operating Conditions for Cyclone IV GX Devices (Part 2 of 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCH_GXB}	Transceiver output buffer power supply	—	2.375	2.5	2.625	V
V_{CCA_GXB}	Transceiver PMA and auxiliary power supply	—	2.375	2.5	2.625	V
V_{CCL_GXB}	Transceiver PMA and auxiliary power supply	—	1.16	1.2	1.24	V
V_I	DC input voltage	—	–0.5	—	3.6	V
V_O	DC output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	For commercial use	0	—	85	°C
		For industrial use	–40	—	100	°C
t_{RAMP}	Power supply ramp time	Standard power-on reset (POR) (7)	50 µs	—	50 ms	—
		Fast POR (8)	50 µs	—	3 ms	—
I_{Diode}	Magnitude of DC current across PCI-clamp diode when enabled	—	—	—	10	mA

Notes to Table 1–4:

(1) All VCCA pins must be powered to 2.5 V (even when PLLs are not used) and must be powered up and powered down at the same time.

(2) You must connect V_{CCD_PLL} to V_{CCINT} through a decoupling capacitor and ferrite bead.

(3) Power supplies must rise monotonically.

(4) V_{CCIO} for all I/O banks must be powered up during device operation. Configurations pins are powered up by V_{CCIO} of I/O Banks 3, 8, and 9 where I/O Banks 3 and 9 only support V_{CCIO} of 1.5, 1.8, 2.5, 3.0, and 3.3 V. For fast passive parallel (FPP) configuration mode, the V_{CCIO} level of I/O Bank 8 must be powered up to 1.5, 1.8, 2.5, 3.0, and 3.3 V.

(5) You must set V_{CC_CLKIN} to 2.5 V if you use CLKIN as a high-speed serial interface (HSSI) refclk or as a DIFFCLK input.

(6) The CLKIN pins in I/O Banks 3B and 8B can support single-ended I/O standard when the pins are used to clock left PLLs in non-transceiver applications.

(7) The POR time for Standard POR ranges between 50 and 200 ms. V_{CCINT}, V_{CCA}, and V_{CCIO} of I/O Banks 3, 8, and 9 must reach the recommended operating range within 50 ms.

(8) The POR time for Fast POR ranges between 3 and 9 ms. V_{CCINT}, V_{CCA}, and V_{CCIO} of I/O Banks 3, 8, and 9 must reach the recommended operating range within 3 ms.

ESD Performance

This section lists the electrostatic discharge (ESD) voltages using the human body model (HBM) and charged device model (CDM) for Cyclone IV devices general purpose I/Os (GPIOs) and high-speed serial interface (HSSI) I/Os. Table 1–5 lists the ESD for Cyclone IV devices GPIOs and HSSI I/Os.

Table 1–5. ESD for Cyclone IV Devices GPIOs and HSSI I/Os

Symbol	Parameter	Passing Voltage	Unit
V_{ESDHBM}	ESD voltage using the HBM (GPIOs) (1)	± 2000	V
	ESD using the HBM (HSSI I/Os) (2)	± 1000	V
V_{ESDCDM}	ESD using the CDM (GPIOs)	± 500	V
	ESD using the CDM (HSSI I/Os) (2)	± 250	V

Notes to Table 1–5:

(1) The passing voltage for EP4CGX15 and EP4CGX30 row I/Os is ±1000V.

(2) This value is applicable only to Cyclone IV GX devices.

DC Characteristics

This section lists the I/O leakage current, pin capacitance, on-chip termination (OCT) tolerance, and bus hold specifications for Cyclone IV devices.

Supply Current

The device supply current requirement is the minimum current drawn from the power supply pins that can be used as a reference for power size planning. Use the Excel-based early power estimator (EPE) to get the supply current estimates for your design because these currents vary greatly with the resources used. Table 1–6 lists the I/O pin leakage current for Cyclone IV devices.

Table 1–6. I/O Pin Leakage Current for Cyclone IV Devices *(1), (2)*

Symbol	Parameter	Conditions	Device	Min	Typ	Max	Unit
I_I	Input pin leakage current	V_I = 0 V to $V_{CCIOMAX}$	—	–10	—	10	µA
I_{OZ}	Tristated I/O pin leakage current	V_O = 0 V to $V_{CCIOMAX}$	—	–10	—	10	µA

Notes to Table 1–6:

(1) This value is specified for normal device operation. The value varies during device power-up. This applies for all V_{CCIO} settings (3.3, 3.0, 2.5, 1.8, 1.5, and 1.2 V).

(2) The 10 µA I/O leakage current limit is applicable when the internal clamping diode is off. A higher current can be observed when the diode is on.

Bus Hold

The bus hold retains the last valid logic state after the source driving it either enters the high impedance state or is removed. Each I/O pin has an option to enable bus hold in user mode. Bus hold is always disabled in configuration mode.

Table 1–7 lists bus hold specifications for Cyclone IV devices.

Table 1–7. Bus Hold Parameter for Cyclone IV Devices (Part 1 of 2) *(1)*

Parameter	Condition	V_{CCIO} (V)												Unit
		1.2		1.5		1.8		2.5		3.0		3.3		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus hold low, sustaining current	$V_{IN} > V_{IL}$ (maximum)	8	—	12	—	30	—	50	—	70	—	70	—	µA
Bus hold high, sustaining current	$V_{IN} < V_{IL}$ (minimum)	–8	—	–12	—	–30	—	–50	—	–70	—	–70	—	µA
Bus hold low, overdrive current	0 V < V_{IN} < V_{CCIO}	—	125	—	175	—	200	—	300	—	500	—	500	µA
Bus hold high, overdrive current	0 V < V_{IN} < V_{CCIO}	—	–125	—	–175	—	–200	—	–300	—	–500	—	–500	µA

Table 1–7. Bus Hold Parameter for Cyclone IV Devices (Part 2 of 2) (1)

Parameter	Condition	V_{CCIO} (V)												Unit
		1.2		1.5		1.8		2.5		3.0		3.3		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus hold trip point	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

Note to Table 1–7:

(1) Bus hold trip points are based on the calculated input voltages from the JEDEC standard.

OCT Specifications

Table 1–8 lists the variation of OCT without calibration across process, temperature, and voltage (PVT).

Table 1–8. Series OCT Without Calibration Specifications for Cyclone IV Devices

Description	V_{CCIO} (V)	Resistance Tolerance		Unit
		Commercial Maximum	Industrial, Extended industrial, and Automotive Maximum	
Series OCT without calibration	3.0	±30	±40	%
	2.5	±30	±40	%
	1.8	±40	±50	%
	1.5	±50	±50	%
	1.2	±50	±50	%

OCT calibration is automatically performed at device power-up for OCT-enabled I/Os.

Table 1–9 lists the OCT calibration accuracy at device power-up.

Table 1–9. Series OCT with Calibration at Device Power-Up Specifications for Cyclone IV Devices

Description	V_{CCIO} (V)	Calibration Accuracy		Unit
		Commercial Maximum	Industrial, Extended industrial, and Automotive Maximum	
Series OCT with calibration at device power-up	3.0	±10	±10	%
	2.5	±10	±10	%
	1.8	±10	±10	%
	1.5	±10	±10	%
	1.2	±10	±10	%

The OCT resistance may vary with the variation of temperature and voltage after calibration at device power-up. Use Table 1–10 and Equation 1–1 to determine the final OCT resistance considering the variations after calibration at device power-up. Table 1–10 lists the change percentage of the OCT resistance with voltage and temperature.

Table 1–10. OCT Variation After Calibration at Device Power-Up for Cyclone IV Devices

Nominal Voltage	dR/dT (%/°C)	dR/dV (%/mV)
3.0	0.262	–0.026
2.5	0.234	–0.039
1.8	0.219	–0.086
1.5	0.199	–0.136
1.2	0.161	–0.288

Equation 1–1. Final OCT Resistance *(1), (2), (3), (4), (5), (6)*

$$\Delta R_V = (V_2 - V_1) \times 1000 \times dR/dV \quad (7)$$

$$\Delta R_T = (T_2 - T_1) \times dR/dT \quad (8)$$

$$\text{For } \Delta R_x < 0;\ MF_x = 1/(|\Delta R_x|/100 + 1) \quad (9)$$

$$\text{For } \Delta R_x > 0;\ MF_x = \Delta R_x/100 + 1 \quad (10)$$

$$MF = MF_V \times MF_T \quad (11)$$

$$R_{final} = R_{initial} \times MF \quad (12)$$

Notes to Equation 1–1:

(1) T_2 is the final temperature.
(2) T_1 is the initial temperature.
(3) MF is multiplication factor.
(4) R_{final} is final resistance.
(5) $R_{initial}$ is initial resistance.
(6) Subscript $_x$ refers to both $_V$ and $_T$.
(7) ΔR_V is a variation of resistance with voltage.
(8) ΔR_T is a variation of resistance with temperature.
(9) dR/dT is the change percentage of resistance with temperature after calibration at device power-up.
(10) dR/dV is the change percentage of resistance with voltage after calibration at device power-up.
(11) V_2 is final voltage.
(12) V_1 is the initial voltage.

Example 1–1 shows how to calculate the change of 50-Ω I/O impedance from 25°C at 3.0 V to 85°C at 3.15 V.

Example 1–1. Impedance Change

$\Delta R_V = (3.15 – 3) \times 1000 \times –0.026 = –3.83$

$\Delta R_T = (85 – 25) \times 0.262 = 15.72$

Because ΔR_V is negative,

$MF_V = 1 / (3.83/100 + 1) = 0.963$

Because ΔR_T is positive,

$MF_T = 15.72/100 + 1 = 1.157$

$MF = 0.963 \times 1.157 = 1.114$

$R_{final} = 50 \times 1.114 = 55.71\ \Omega$

Pin Capacitance

Table 1–11 lists the pin capacitance for Cyclone IV devices.

Table 1–11. Pin Capacitance for Cyclone IV Devices *(1)*

Symbol	Parameter	Typical – Quad Flat Pack (QFP)	Typical – Quad Flat No Leads (QFN)	Typical – Ball-Grid Array (BGA)	Unit
C_{IOTB}	Input capacitance on top and bottom I/O pins	7	7	6	pF
C_{IOLR}	Input capacitance on right I/O pins	7	7	5	pF
C_{LVDSLR}	Input capacitance on right I/O pins with dedicated LVDS output	8	8	7	pF
C_{VREFLR} *(2)*	Input capacitance on right dual-purpose VREF pin when used as V_{REF} or user I/O pin	21	21	21	pF
C_{VREFTB} *(2)*	Input capacitance on top and bottom dual-purpose VREF pin when used as V_{REF} or user I/O pin	23 *(3)*	23	23	pF
C_{CLKTB}	Input capacitance on top and bottom dedicated clock input pins	7	7	6	pF
C_{CLKLR}	Input capacitance on right dedicated clock input pins	6	6	5	pF

Notes to Table 1–11:

(1) The pin capacitance applies to FBGA, UBGA, and MBGA packages.

(2) When you use the VREF pin as a regular input or output, you can expect a reduced performance of toggle rate and t_{CO} because of higher pin capacitance.

(3) C_{VREFTB} for the EP4CE22 device is 30 pF.

Internal Weak Pull-Up and Weak Pull-Down Resistor

Table 1–12 lists the weak pull-up and pull-down resistor values for Cyclone IV devices.

Table 1–12. Internal Weak Pull-Up and Weak Pull-Down Resistor Values for Cyclone IV Devices *(1)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{_PU}$	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option	V_{CCIO} = 3.3 V ± 5% *(2), (3)*	7	25	41	kΩ
		V_{CCIO} = 3.0 V ± 5% *(2), (3)*	7	28	47	kΩ
		V_{CCIO} = 2.5 V ± 5% *(2), (3)*	8	35	61	kΩ
		V_{CCIO} = 1.8 V ± 5% *(2), (3)*	10	57	108	kΩ
		V_{CCIO} = 1.5 V ± 5% *(2), (3)*	13	82	163	kΩ
		V_{CCIO} = 1.2 V ± 5% *(2), (3)*	19	143	351	kΩ
$R_{_PD}$	Value of the I/O pin pull-down resistor before and during configuration	V_{CCIO} = 3.3 V ± 5% *(4)*	6	19	30	kΩ
		V_{CCIO} = 3.0 V ± 5% *(4)*	6	22	36	kΩ
		V_{CCIO} = 2.5 V ± 5% *(4)*	6	25	43	kΩ
		V_{CCIO} = 1.8 V ± 5% *(4)*	7	35	71	kΩ
		V_{CCIO} = 1.5 V ± 5% *(4)*	8	50	112	kΩ

Notes to Table 1–12:

(1) All I/O pins have an option to enable weak pull-up except the configuration, test, and JTAG pins. The weak pull-down feature is only available for JTAG TCK.

(2) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

(3) $R_{_PU} = (V_{CCIO} – V_I)/I_{R_PU}$
Minimum condition: –40°C; $V_{CCIO} = V_{CC}$ + 5%, $V_I = V_{CC}$ + 5% – 50 mV;
Typical condition: 25°C; $V_{CCIO} = V_{CC}$, V_I = 0 V;
Maximum condition: 100°C; $V_{CCIO} = V_{CC}$ – 5%, V_I = 0 V; in which V_I refers to the input voltage at the I/O pin.

(4) $R_{_PD} = V_I/I_{R_PD}$
Minimum condition: –40°C; $V_{CCIO} = V_{CC}$ + 5%, V_I = 50 mV;
Typical condition: 25°C; $V_{CCIO} = V_{CC}$, $V_I = V_{CC}$ – 5%;
Maximum condition: 100°C; $V_{CCIO} = V_{CC}$ – 5%, $V_I = V_{CC}$ – 5%; in which V_I refers to the input voltage at the I/O pin.

Hot-Socketing

Table 1–13 lists the hot-socketing specifications for Cyclone IV devices.

Table 1–13. Hot-Socketing Specifications for Cyclone IV Devices

Symbol	Parameter	Maximum
$I_{IOPIN(DC)}$	DC current per I/O pin	300 µA
$I_{IOPIN(AC)}$	AC current per I/O pin	8 mA *(1)*
$I_{XCVRTX(DC)}$	DC current per transceiver TX pin	100 mA
$I_{XCVRRX(DC)}$	DC current per transceiver RX pin	50 mA

Note to Table 1–13:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, |IIOPIN| = C dv/dt, in which C is the I/O pin capacitance and dv/dt is the slew rate.

During hot-socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF.

Schmitt Trigger Input

Cyclone IV devices support Schmitt trigger input on the TDI, TMS, TCK, nSTATUS, nCONFIG, nCE, CONF_DONE, and DCLK pins. A Schmitt trigger feature introduces hysteresis to the input signal for improved noise immunity, especially for signals with slow edge rate. Table 1–14 lists the hysteresis specifications across the supported V_{CCIO} range for Schmitt trigger inputs in Cyclone IV devices.

Table 1–14. Hysteresis Specifications for Schmitt Trigger Input in Cyclone IV Devices

Symbol	Parameter	Conditions (V)	Minimum	Unit
$V_{SCHMITT}$	Hysteresis for Schmitt trigger input	V_{CCIO} = 3.3	200	mV
		V_{CCIO} = 2.5	200	mV
		V_{CCIO} = 1.8	140	mV
		V_{CCIO} = 1.5	110	mV

I/O Standard Specifications

The following tables list input voltage sensitivities (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}), for various I/O standards supported by Cyclone IV devices. Table 1–15 through Table 1–20 provide the I/O standard specifications for Cyclone IV devices.

Table 1–15. Single-Ended I/O Standard Specifications for Cyclone IV Devices (1), (2)

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA) (4)	I_{OH} (mA) (4)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3-V LVTTL (3)	3.135	3.3	3.465	—	0.8	1.7	3.6	0.45	2.4	4	–4
3.3-V LVCMOS (3)	3.135	3.3	3.465	—	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	2	–2
3.0-V LVTTL (3)	2.85	3.0	3.15	–0.3	0.8	1.7	V_{CCIO} + 0.3	0.45	2.4	4	–4
3.0-V LVCMOS (3)	2.85	3.0	3.15	–0.3	0.8	1.7	V_{CCIO} + 0.3	0.2	V_{CCIO} – 0.2	0.1	–0.1
2.5 V (3)	2.375	2.5	2.625	–0.3	0.7	1.7	V_{CCIO} + 0.3	0.4	2.0	1	–1
1.8 V	1.71	1.8	1.89	–0.3	0.35 x V_{CCIO}	0.65 x V_{CCIO}	2.25	0.45	V_{CCIO} – 0.45	2	–2
1.5 V	1.425	1.5	1.575	–0.3	0.35 x V_{CCIO}	0.65 x V_{CCIO}	V_{CCIO} + 0.3	0.25 x V_{CCIO}	0.75 x V_{CCIO}	2	–2
1.2 V	1.14	1.2	1.26	–0.3	0.35 x V_{CCIO}	0.65 x V_{CCIO}	V_{CCIO} + 0.3	0.25 x V_{CCIO}	0.75 x V_{CCIO}	2	–2
3.0-V PCI	2.85	3.0	3.15	—	0.3 x V_{CCIO}	0.5 x V_{CCIO}	V_{CCIO} + 0.3	0.1 x V_{CCIO}	0.9 x V_{CCIO}	1.5	–0.5
3.0-V PCI-X	2.85	3.0	3.15	—	0.35 x V_{CCIO}	0.5 x V_{CCIO}	V_{CCIO} + 0.3	0.1 x V_{CCIO}	0.9 x V_{CCIO}	1.5	–0.5

Notes to Table 1–15:

(1) For voltage-referenced receiver input waveform and explanation of terms used in Table 1–15, refer to "Glossary" on page 1–37.

(2) AC load CL = 10 pF

(3) For more information about interfacing Cyclone IV devices with 3.3/3.0/2.5-V LVTTL/LVCMOS I/O standards, refer to *AN 447: Interfacing Cyclone III and Cyclone IV Devices with 3.3/3.0/2.5-V LVTTL/LVCMOS I/O Systems*.

(4) To meet the I_{OL} and I_{OH} specifications, you must set the current strength settings accordingly. For example, to meet the **3.3-V LVTTL** specification (4 mA), set the current strength settings to 4 mA or higher. Setting at lower current strength may not meet the I_{OL} and I_{OH} specifications in the handbook.

Table 1–16. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications for Cyclone IV Devices *(1)*

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V) *(2)*		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	1.19	1.25	1.31	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.7	1.8	1.9	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	0.85	0.9	0.95
HSTL-15 Class I, II	1.425	1.5	1.575	0.71	0.75	0.79	0.71	0.75	0.79
HSTL-12 Class I, II	1.14	1.2	1.26	0.48 x V_{CCIO} *(3)* 0.47 x V_{CCIO} *(4)*	0.5 x V_{CCIO} *(3)* 0.5 x V_{CCIO} *(4)*	0.52 x V_{CCIO} *(3)* 0.53 x V_{CCIO} *(4)*	—	0.5 x V_{CCIO}	—

Notes to Table 1–16:

(1) For an explanation of terms used in Table 1–16, refer to "Glossary" on page 1–37.
(2) V_{TT} of the transmitting device must track V_{REF} of the receiving device.
(3) Value shown refers to DC input reference voltage, $V_{REF(DC)}$.
(4) Value shown refers to AC input reference voltage, $V_{REF(AC)}$.

Table 1–17. Single-Ended SSTL and HSTL I/O Standards Signal Specifications for Cyclone IV Devices

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)		$V_{IH(AC)}$ (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Max	Min	Max	Min	Max	Min	Max	Max	Min		
SSTL-2 Class I	—	V_{REF} – 0.18	V_{REF} + 0.18	—	—	V_{REF} – 0.35	V_{REF} + 0.35	—	V_{TT} – 0.57	V_{TT} + 0.57	8.1	–8.1
SSTL-2 Class II	—	V_{REF} – 0.18	V_{REF} + 0.18	—	—	V_{REF} – 0.35	V_{REF} + 0.35	—	V_{TT} – 0.76	V_{TT} + 0.76	16.4	–16.4
SSTL-18 Class I	—	V_{REF} – 0.125	V_{REF} + 0.125	—	—	V_{REF} – 0.25	V_{REF} + 0.25	—	V_{TT} – 0.475	V_{TT} + 0.475	6.7	–6.7
SSTL-18 Class II	—	V_{REF} – 0.125	V_{REF} + 0.125	—	—	V_{REF} – 0.25	V_{REF} + 0.25	—	0.28	V_{CCIO} – 0.28	13.4	–13.4
HSTL-18 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	—	V_{REF} – 0.2	V_{REF} + 0.2	—	0.4	V_{CCIO} – 0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	–0.24	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.24	0.25 × V_{CCIO}	0.75 × V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	–0.24	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.24	0.25 × V_{CCIO}	0.75 × V_{CCIO}	14	–14

For more information about receiver input and transmitter output waveforms, and for other differential I/O standards, refer to the *I/O Features in Cyclone IV Devices* chapter.

Table 1–18. Differential SSTL I/O Standard Specifications for Cyclone IV Devices *(1)*

I/O Standard	V_{CCIO} (V)			$V_{Swing(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{Swing(AC)}$ (V)		$V_{OX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.36	V_{CCIO}	$V_{CCIO}/2 - 0.2$	—	$V_{CCIO}/2 + 0.2$	0.7	V_{CCIO}	$V_{CCIO}/2 - 0.125$	—	$V_{CCIO}/2 + 0.125$
SSTL-18 Class I, II	1.7	1.8	1.90	0.25	V_{CCIO}	$V_{CCIO}/2 - 0.175$	—	$V_{CCIO}/2 + 0.175$	0.5	V_{CCIO}	$V_{CCIO}/2 - 0.125$	—	$V_{CCIO}/2 + 0.125$

Note to Table 1–18:

(1) Differential SSTL requires a V_{REF} input.

Table 1–19. Differential HSTL I/O Standard Specifications for Cyclone IV Devices *(1)*

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.85	—	0.95	0.85	—	0.95	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.71	—	0.79	0.71	—	0.79	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO}	$0.48 \times V_{CCIO}$	—	$0.52 \times V_{CCIO}$	$0.48 \times V_{CCIO}$	—	$0.52 \times V_{CCIO}$	0.3	$0.48 \times V_{CCIO}$

Note to Table 1–19:

(1) Differential HSTL requires a V_{REF} input.

Table 1–20. Differential I/O Standard Specifications for Cyclone IV Devices *(1)* **(Part 1 of 2)**

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)		V_{ICM} (V) *(2)*			V_{OD} (mV) *(3)*			V_{OS} (V) *(3)*		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVPECL (Row I/Os) *(6)*	2.375	2.5	2.625	100	—	0.05	$D_{MAX} \leq 500$ Mbps	1.80	—	—	—	—	—	—
						0.55	500 Mbps $\leq D_{MAX} \leq$ 700 Mbps	1.80						
						1.05	$D_{MAX} >$ 700 Mbps	1.55						
LVPECL (Column I/Os) *(6)*	2.375	2.5	2.625	100	—	0.05	$D_{MAX} \leq$ 500 Mbps	1.80	—	—	—	—	—	—
						0.55	500 Mbps $\leq D_{MAX} \leq$ 700 Mbps	1.80						
						1.05	$D_{MAX} >$ 700 Mbps	1.55						
LVDS (Row I/Os)	2.375	2.5	2.625	100	—	0.05	$D_{MAX} \leq 500$ Mbps	1.80	247	—	600	1.125	1.25	1.375
						0.55	500 Mbps $\leq D_{MAX} \leq$ 700 Mbps	1.80						
						1.05	$D_{MAX} >$ 700 Mbps	1.55						

Table 1–20. Differential I/O Standard Specifications for Cyclone IV Devices (1) (Part 2 of 2)

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)		V_{ICM} (V) (2)			V_{OD} (mV) (3)			V_{OS} (V) (3)		
	Min	Typ	Max	Min	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
LVDS (Column I/Os)	2.375	2.5	2.625	100	—	0.05	$D_{MAX} \leq$ 500 Mbps	1.80	247	—	600	1.125	1.25	1.375
						0.55	500 Mbps $\leq D_{MAX} \leq$ 700 Mbps	1.80						
						1.05	D_{MAX} > 700 Mbps	1.55						
BLVDS (Row I/Os) (4)	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—
BLVDS (Column I/Os) (4)	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—
mini-LVDS (Row I/Os) (5)	2.375	2.5	2.625	—	—	—	—	—	300	—	600	1.0	1.2	1.4
mini-LVDS (Column I/Os) (5)	2.375	2.5	2.625	—	—	—	—	—	300	—	600	1.0	1.2	1.4
RSDS® (Row I/Os) (5)	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.5
RSDS (Column I/Os) (5)	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.5
PPDS (Row I/Os) (5)	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.4
PPDS (Column I/Os) (5)	2.375	2.5	2.625	—	—	—	—	—	100	200	600	0.5	1.2	1.4

Notes to Table 1–20:

(1) For an explanation of terms used in Table 1–20, refer to "Glossary" on page 1–37.
(2) V_{IN} range: 0 V $\leq V_{IN} \leq$ 1.85 V.
(3) R_L range: 90 $\leq R_L \leq$ 110 Ω.
(4) There are no fixed V_{IN}, V_{OD}, and V_{OS} specifications for BLVDS. They depend on the system topology.
(5) The Mini-LVDS, RSDS, and PPDS standards are only supported at the output pins.
(6) The LVPECL I/O standard is only supported on dedicated clock input pins. This I/O standard is not supported for output pins.

Power Consumption

Use the following methods to estimate power for a design:

- the Excel-based EPE
- the Quartus® II PowerPlay power analyzer feature

The interactive Excel-based EPE is used prior to designing the device to get a magnitude estimate of the device power. The Quartus II PowerPlay power analyzer provides better quality estimates based on the specifics of the design after place-and-route is complete. The PowerPlay power analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, combined with detailed circuit models, can yield very accurate power estimates.

For more information about power estimation tools, refer to the *Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

Switching Characteristics

This section provides performance characteristics of Cyclone IV core and periphery blocks for commercial grade devices.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The upper-right hand corner of these tables show the designation as “Preliminary”.
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

Transceiver Performance Specifications

Table 1–21 lists the Cyclone IV GX transceiver specifications.

Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 1 of 4)

Symbol/ Description	Conditions	C6			C7, I7			C8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Clock											
Supported I/O Standards	1.2 V PCML, 1.5 V PCML, 3.3 V PCML, Differential LVPECL, LVDS, HCSL										
Input frequency from REFCLK input pins	—	50	—	156.25	50	—	156.25	50	—	156.25	MHz
Spread-spectrum modulating clock frequency	Physical interface for PCI Express (PIPE) mode	30	—	33	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PIPE mode	—	0 to –0.5%	—	—	0 to –0.5%	—	—	0 to –0.5%	—	—
Peak-to-peak differential input voltage	—	0.1	—	1.6	0.1	—	1.6	0.1	—	1.6	V
V_{ICM} (AC coupled)	—	1100 ± 5%			1100 ± 5%			1100 ± 5%			mV
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	250	—	550	mV
Transmitter REFCLK Phase Noise (1)	Frequency offset = 1 MHz – 8 MHZ	—	—	–123	—	—	–123	—	—	–123	dBc/Hz
Transmitter REFCLK Total Jitter (1)		—	—	42.3	—	—	42.3	—	—	42.3	ps
R_{ref}	—	—	2000 ± 1%	—	—	2000 ± 1%	—	—	2000 ± 1%	—	Ω
Transceiver Clock											
cal_blk_clk clock frequency	—	10	—	125	10	—	125	10	—	125	MHz
fixedclk clock frequency	PCIe Receiver Detect	—	125	—	—	125	—	—	125	—	MHz
reconfig_clk clock frequency	Dynamic reconfiguration clock frequency	2.5/ 37.5 (2)	—	50	2.5/ 37.5 (2)	—	50	2.5/ 37.5 (2)	—	50	MHz
Delta time between reconfig_clk	—	—	—	2	—	—	2	—	—	2	ms
Transceiver block minimum power-down pulse width	—	—	1	—	—	1	—	—	1	—	µs

Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 2 of 4)

Symbol/ Description	Conditions	C6			C7, I7			C8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Receiver											
Supported I/O Standards	1.4 V PCML, 1.5 V PCML, 2.5 V PCML, LVPECL, LVDS										
Data rate (F324 and smaller package) (15)	—	600	—	2500	600	—	2500	600	—	2500	Mbps
Data rate (F484 and larger package) (15)	—	600	—	3125	600	—	3125	600	—	2500	Mbps
Absolute V_{MAX} for a receiver pin (3)	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Operational V_{MAX} for a receiver pin	—	—	—	1.5	—	—	1.5	—	—	1.5	V
Absolute V_{MIN} for a receiver pin	—	–0.4	—	—	–0.4	—	—	–0.4	—	—	V
Peak-to-peak differential input voltage V_{ID} (diff p-p)	V_{ICM} = 0.82 V setting, Data Rate = 600 Mbps to 3.125 Gbps	0.1	—	2.7	0.1	—	2.7	0.1	—	2.7	V
V_{ICM}	V_{ICM} = 0.82 V setting	—	820 ± 10%	—	—	820 ± 10%	—	—	820 ± 10%	—	mV
Differential on-chip termination resistors	100–Ω setting	—	100	—	—	100	—	—	100	—	Ω
	150–Ω setting	—	150	—	—	150	—	—	150	—	Ω
Differential and common mode return loss	PIPE, Serial Rapid I/O SR, SATA, CPRI LV, SDI, XAUI	Compliant									—
Programmable ppm detector (4)	—	± 62.5, 100, 125, 200, 250, 300									ppm
Clock data recovery (CDR) ppm tolerance (without spread-spectrum clocking enabled)	—	—	—	±300 (5), ±350 (6), (7)	—	—	±300 (5), ±350 (6), (7)	—	—	±300 (5), ±350 (6), (7)	ppm
CDR ppm tolerance (with synchronous spread-spectrum clocking enabled) (8)	—	—	—	350 to –5350 (7), (9)	—	—	350 to –5350 (7), (9)	—	—	350 to –5350 (7), (9)	ppm
Run length	—	—	80	—	—	80	—	—	80	—	UI
Programmable equalization	No Equalization	—	—	1.5	—	—	1.5	—	—	1.5	dB
	Medium Low	—	—	4.5	—	—	4.5	—	—	4.5	dB
	Medium High	—	—	5.5	—	—	5.5	—	—	5.5	dB
	High	—	—	7	—	—	7	—	—	7	dB

Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 3 of 4)

Symbol/ Description	Conditions	C6			C7, I7			C8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Signal detect/loss threshold	PIPE mode	65	—	175	65	—	175	65	—	175	mV
t_{LTR} (10)	—	—	—	75	—	—	75	—	—	75	µs
$t_{LTR-LTD_Manual}$ (11)	—	15	—	—	15	—	—	15	—	—	µs
t_{LTD} (12)	—	0	100	4000	0	100	4000	0	100	4000	ns
t_{LTD_Manual} (13)	—	—	—	4000	—	—	4000	—	—	4000	ns
t_{LTD_Auto} (14)	—	—	—	4000	—	—	4000	—	—	4000	ns
Receiver buffer and CDR offset cancellation time (per channel)	—	—	—	17000	—	—	17000	—	—	17000	reconfig_clk cycles
Programmable DC gain	DC Gain Setting = 0	—	0	—	—	0	—	—	0	—	dB
	DC Gain Setting = 1	—	3	—	—	3	—	—	3	—	dB
	DC Gain Setting = 2	—	6	—	—	6	—	—	6	—	dB
Transmitter											
Supported I/O Standards	1.5 V PCML										
Data rate (F324 and smaller package)	—	600	—	2500	600	—	2500	600	—	2500	Mbps
Data rate (F484 and larger package)	—	600	—	3125	600	—	3125	600	—	2500	Mbps
V_{OCM}	0.65 V setting	—	650	—	—	650	—	—	650	—	mV
Differential on-chip termination resistors	100–Ω setting	—	100	—	—	100	—	—	100	—	Ω
	150–Ω setting	—	150	—	—	150	—	—	150	—	Ω
Differential and common mode return loss	PIPE, CPRI LV, Serial Rapid I/O SR, SDI, XAUI, SATA	Compliant									—
Rise time	—	50	—	200	50	—	200	50	—	200	ps
Fall time	—	50	—	200	50	—	200	50	—	200	ps
Intra-differential pair skew	—	—	—	15	—	—	15	—	—	15	ps
Intra-transceiver block skew	—	—	—	120	—	—	120	—	—	120	ps

Table 1–21. Transceiver Specification for Cyclone IV GX Devices (Part 4 of 4)

Symbol/ Description	Conditions	C6			C7, I7			C8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
PLD-Transceiver Interface											
Interface speed (F324 and smaller package)	—	25	—	125	25	—	125	25	—	125	MHz
Interface speed (F484 and larger package)	—	25	—	156.25	25	—	156.25	25	—	156.25	MHz
Digital reset pulse width	—	Minimum is 2 parallel clock cycles									

Notes to Table 1–21:

(1) This specification is valid for transmitter output jitter specification with a maximum total jitter value of 112 ps, typically for 3.125 Gbps SRIO and XAUI protocols.

(2) The minimum `reconfig_clk` frequency is 2.5 MHz if the transceiver channel is configured in **Transmitter Only** mode. The minimum `reconfig_clk` frequency is 37.5 MHz if the transceiver channel is configured in **Receiver Only** or **Receiver and Transmitter** mode.

(3) The device cannot tolerate prolonged operation at this absolute maximum.

(4) The rate matcher supports only up to ±300 parts per million (ppm).

(5) Supported for the N148, F169, and F324 device packages only.

(6) Supported for the F484, F672, and F896 device packages only. Pending device characterization.

(7) To support CDR ppm tolerance greater than ±300 ppm, implement ppm detector in user logic and configure CDR to Manual Lock Mode.

(8) Asynchronous spread-spectrum clocking is not supported.

(9) For the EP4CGX30 (F484 package only), EP4CGX50, and EP4CGX75 devices, the CDR ppl tolerance is ±200 ppm.

(10) Time taken until `pll_locked` goes high after `pll_powerdown` deasserts.

(11) Time that the CDR must be kept in lock-to-reference mode after `rx_analogreset` deasserts and before `rx_locktodata` is asserted in manual mode.

(12) Time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode (Figure 1–2), or after `rx_freqlocked` signal goes high in automatic mode (Figure 1–3).

(13) Time taken to recover valid data after the `rx_locktodata` signal is asserted in manual mode.

(14) Time taken to recover valid data after the `rx_freqlocked` signal goes high in automatic mode.

(15) To support data rates lower than the minimum specification through oversampling, use the CDR in LTR mode only.

Figure 1–2 shows the lock time parameters in manual mode.

LTD = lock-to-data. LTR = lock-to-reference.

Figure 1–2. Lock Time Parameters for Manual Mode

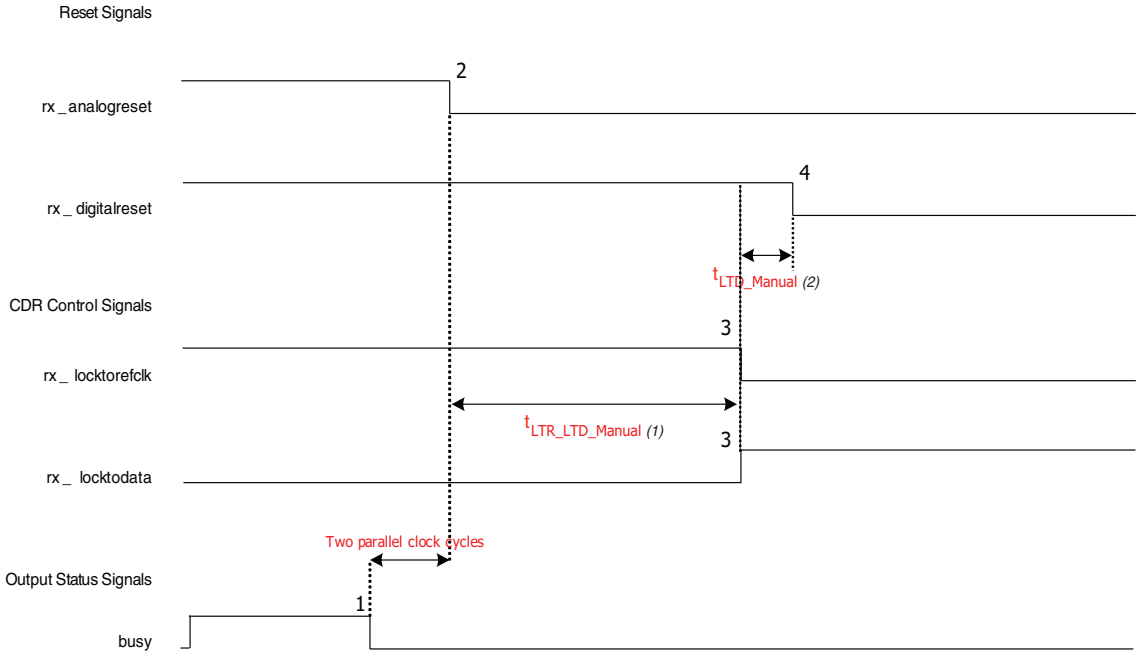


Figure 1–3 shows the lock time parameters in automatic mode.

Figure 1–3. Lock Time Parameters for Automatic Mode

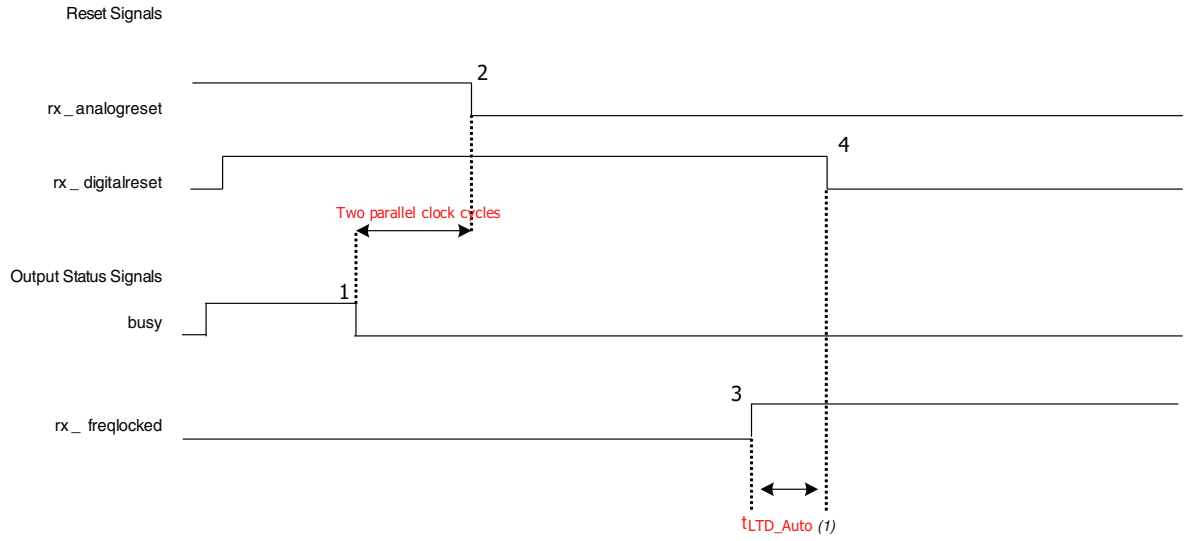


Figure 1–4 shows the differential receiver input waveform.

Figure 1–4. Receiver Input Waveform

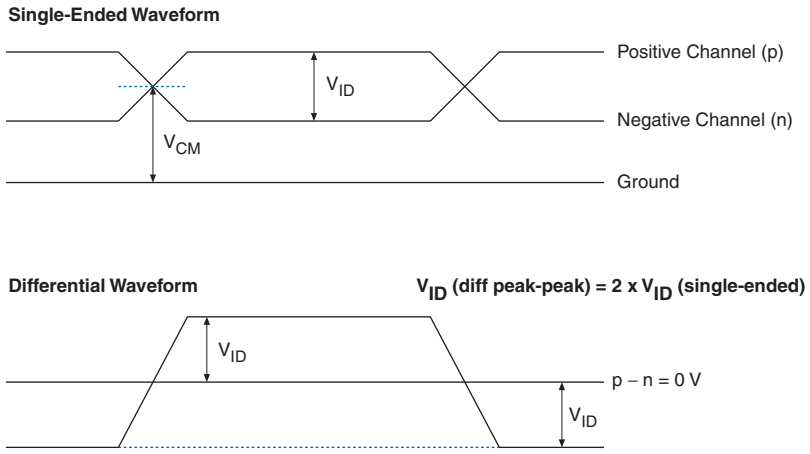


Figure 1–5 shows the transmitter output waveform.

Figure 1–5. Transmitter Output Waveform

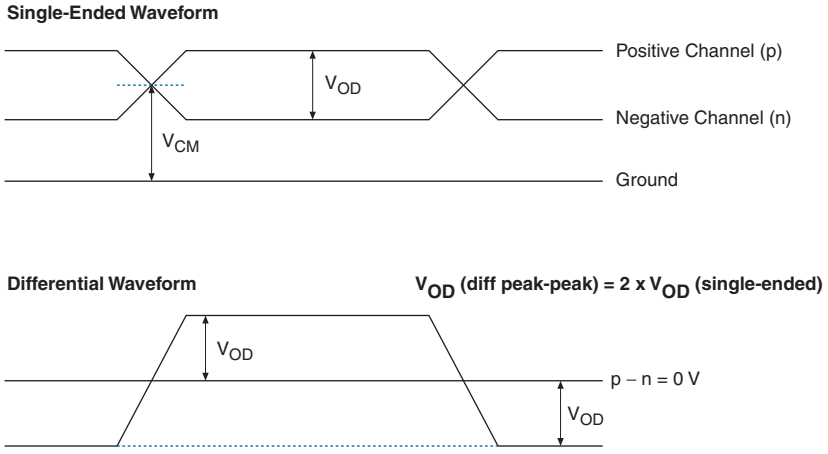


Table 1–22 lists the typical V_{OD} for Tx term that equals 100 Ω.

Table 1–22. Typical V_{OD} Setting, Tx Term = 100 Ω

Symbol	V_{OD} Setting (mV)					
	1	2	3	4 (1)	5	6
V_{OD} differential peak to peak typical (mV)	400	600	800	900	1000	1200

Note to Table 1–22:

(1) This setting is required for compliance with the PCIe protocol.

Table 1–23 lists the Cyclone IV GX transceiver block AC specifications.

Table 1–23. Transceiver Block AC Specification for Cyclone IV GX Devices *(1), (2)*

Symbol/ Description	Conditions	C6			C7, I7			C8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
PCIe Transmit Jitter Generation *(3)*											
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern	—	—	0.25	—	—	0.25	—	—	0.25	UI
PCIe Receiver Jitter Tolerance *(3)*											
Total jitter at 2.5 Gbps (Gen1)	Compliance pattern	> 0.6			> 0.6			> 0.6			UI
GIGE Transmit Jitter Generation *(4)*											
Deterministic jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.14	—	—	0.14	—	—	0.14	UI
Total jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.279	—	—	0.279	—	—	0.279	UI
GIGE Receiver Jitter Tolerance *(4)*											
Deterministic jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.4			> 0.4			> 0.4			UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.66			> 0.66			> 0.66			UI

Notes to Table 1–23:

(1) Dedicated `refclk` pins were used to drive the input reference clocks.
(2) The jitter numbers specified are valid for the stated conditions only.
(3) The jitter numbers for PIPE are compliant to the PCIe Base Specification 2.0.
(4) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.

Core Performance Specifications

The following sections describe the clock tree specifications, PLLs, embedded multiplier, memory block, and configuration specifications for Cyclone IV Devices.

Clock Tree Specifications

Table 1–24 lists the clock tree specifications for Cyclone IV devices.

Table 1–24. Clock Tree Performance for Cyclone IV Devices ***(Part 1 of 2)***

Device	Performance								Unit
	C6	C7	C8	C8L *(1)*	C9L *(1)*	I7	I8L *(1)*	A7	
EP4CE6	500	437.5	402	362	265	437.5	362	402	MHz
EP4CE10	500	437.5	402	362	265	437.5	362	402	MHz
EP4CE15	500	437.5	402	362	265	437.5	362	402	MHz
EP4CE22	500	437.5	402	362	265	437.5	362	402	MHz
EP4CE30	500	437.5	402	362	265	437.5	362	402	MHz
EP4CE40	500	437.5	402	362	265	437.5	362	402	MHz

Table 1–24. Clock Tree Performance for Cyclone IV Devices *(Part 2 of 2)*

Device	Performance								Unit
	C6	C7	C8	C8L (1)	C9L (1)	I7	I8L (1)	A7	
EP4CE55	500	437.5	402	362	265	437.5	362	—	MHz
EP4CE75	500	437.5	402	362	265	437.5	362	—	MHz
EP4CE115	—	437.5	402	362	265	437.5	362	—	MHz
EP4CGX15	500	437.5	402	—	—	437.5	—	—	MHz
EP4CGX22	500	437.5	402	—	—	437.5	—	—	MHz
EP4CGX30	500	437.5	402	—	—	437.5	—	—	MHz
EP4CGX50	500	437.5	402	—	—	437.5	—	—	MHz
EP4CGX75	500	437.5	402	—	—	437.5	—	—	MHz
EP4CGX110	500	437.5	402	—	—	437.5	—	—	MHz
EP4CGX150	500	437.5	402	—	—	437.5	—	—	MHz

Note to Table 1–24:

(1) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades.

PLL Specifications

Table 1–25 lists the PLL specifications for Cyclone IV devices when operating in the commercial junction temperature range (0°C to 85°C), the industrial junction temperature range (–40°C to 100°C), the extended industrial junction temperature range (–40°C to 125°C), and the automotive junction temperature range (–40°C to 125°C). For more information about the PLL block, refer to "Glossary" on page 1–37.

Table 1–25. PLL Specifications for Cyclone IV Devices (1), (2) (Part 1 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN} (3)	Input clock frequency (–6, –7, –8 speed grades)	5	—	472.5	MHz
	Input clock frequency (–8L speed grade)	5	—	362	MHz
	Input clock frequency (–9L speed grade)	5	—	265	MHz
f_{INPFD}	PFD input frequency	5	—	325	MHz
f_{VCO} (4)	PLL internal VCO operating range	600	—	1300	MHz
f_{INDUTY}	Input clock duty cycle	40	—	60	%
$t_{INJITTER_CCJ}$ (5)	Input clock cycle-to-cycle jitter $F_{REF} \geq 100$ MHz	—	—	0.15	UI
	$F_{REF} < 100$ MHz	—	—	±750	ps
f_{OUT_EXT} (external clock output) (3)	PLL output frequency	—	—	472.5	MHz
f_{OUT} (to global clock)	PLL output frequency (–6 speed grade)	—	—	472.5	MHz
	PLL output frequency (–7 speed grade)	—	—	450	MHz
	PLL output frequency (–8 speed grade)	—	—	402.5	MHz
	PLL output frequency (–8L speed grade)	—	—	362	MHz
	PLL output frequency (–9L speed grade)	—	—	265	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	50	55	%
t_{LOCK}	Time required to lock from end of device configuration	—	—	1	ms

Table 1–25. PLL Specifications for Cyclone IV Devices (1), (2) (Part 2 of 2)

Symbol	Parameter	Min	Typ	Max	Unit
t_{DLOCK}	Time required to lock dynamically (after switchover, reconfiguring any non-post-scale counters/delays or areset is deasserted)	—	—	1	ms
$t_{OUTJITTER_PERIOD_DEDCLK}$ (6)	Dedicated clock output period jitter $F_{OUT} \geq 100$ MHz	—	—	300	ps
	$F_{OUT} < 100$ MHz	—	—	30	mUI
$t_{OUTJITTER_CCJ_DEDCLK}$ (6)	Dedicated clock output cycle-to-cycle jitter $F_{OUT} \geq 100$ MHz	—	—	300	ps
	$F_{OUT} < 100$ MHz	—	—	30	mUI
$t_{OUTJITTER_PERIOD_IO}$ (6)	Regular I/O period jitter $F_{OUT} \geq 100$ MHz	—	—	650	ps
	$F_{OUT} < 100$ MHz	—	—	75	mUI
$t_{OUTJITTER_CCJ_IO}$ (6)	Regular I/O cycle-to-cycle jitter $F_{OUT} \geq 100$ MHz	—	—	650	ps
	$F_{OUT} < 100$ MHz	—	—	75	mUI
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±50	ps
t_{ARESET}	Minimum pulse width on areset signal.	10	—	—	ns
$t_{CONFIGPLL}$	Time required to reconfigure scan chains for PLLs	—	3.5 (7)	—	SCANCLK cycles
$f_{SCANCLK}$	scanclk frequency	—	—	100	MHz
$t_{CASC_OUTJITTER_PERIOD_DEDCLK}$ (8), (9)	Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \geq 100$ MHz)	—	—	425	ps
	Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} < 100$ MHz)	—	—	42.5	mUI

Notes to Table 1–25:

(1) This table is applicable for general purpose PLLs and multipurpose PLLs.

(2) You must connect V_{CCD_PLL} to V_{CCINT} through the decoupling capacitor and ferrite bead.

(3) This parameter is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(4) The V_{CO} frequency reported by the Quartus II software in the PLL Summary section of the compilation report takes into consideration the V_{CO} post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f_{VCO} specification.

(5) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source that is less than 200 ps.

(6) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.99999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL when an input jitter of 30 ps is applied.

(7) With 100-MHz scanclk frequency.

(8) The cascaded PLLs specification is applicable only with the following conditions:

- Upstream PLL—0.59 MHz ≤ Upstream PLL bandwidth < 1 MHz
- Downstream PLL—Downstream PLL bandwidth > 2 MHz

(9) PLL cascading is not supported for transceiver applications.

Embedded Multiplier Specifications

Table 1–26 lists the embedded multiplier specifications for Cyclone IV devices.

Table 1–26. Embedded Multiplier Specifications for Cyclone IV Devices

Mode	Resources Used	Performance					Unit
	Number of Multipliers	C6	C7, I7, A7	C8	C8L, I8L	C9L	
9 × 9-bit multiplier	1	340	300	260	240	175	MHz
18 × 18-bit multiplier	1	287	250	200	185	135	MHz

Memory Block Specifications

Table 1–27 lists the M9K memory block specifications for Cyclone IV devices.

Table 1–27. Memory Block Performance Specifications for Cyclone IV Devices

Memory	Mode	Resources Used		Performance					Unit
		LEs	M9K Memory	C6	C7, I7, A7	C8	C8L, I8L	C9L	
M9K Block	FIFO 256 × 36	47	1	315	274	238	200	157	MHz
	Single-port 256 × 36	0	1	315	274	238	200	157	MHz
	Simple dual-port 256 × 36 CLK	0	1	315	274	238	200	157	MHz
	True dual port 512 × 18 single CLK	0	1	315	274	238	200	157	MHz

Configuration and JTAG Specifications

Table 1–28 lists the configuration mode specifications for Cyclone IV devices.

Table 1–28. Passive Configuration Mode Specifications for Cyclone IV Devices (1)

Programming Mode	V_{CCINT} Voltage Level (V)	DCLK f_{MAX}	Unit
Passive Serial (PS)	1.0 (3)	66	MHz
	1.2	133	MHz
Fast Passive Parallel (FPP) (2)	1.0 (3)	66	MHz
	1.2 (4)	100	MHz

Notes to Table 1–28:

(1) For more information about PS and FPP configuration timing parameters, refer to the *Configuration and Remote System Upgrades in Cyclone IV Devices* chapter.

(2) FPP configuration mode supports all Cyclone IV E devices (except for E144 package devices) and EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 only.

(3) V_{CCINT} = 1.0 V is only supported for Cyclone IV E 1.0 V core voltage devices.

(4) Cyclone IV E devices support 1.2 V V_{CCINT}. Cyclone IV E 1.2 V core voltage devices support 133 MHz DCLK f_{MAX} for EP4CE6, EP4CE10, EP4CE15, EP4CE22, EP4CE30, and EP4CE40 only.

Table 1–29 lists the active configuration mode specifications for Cyclone IV devices.

Table 1–29. Active Configuration Mode Specifications for Cyclone IV Devices

Programming Mode	DCLK Range	Typical DCLK	Unit
Active Parallel (AP) (1)	20 to 40	33	MHz
Active Serial (AS)	20 to 40	33	MHz

Note to Table 1–29:

(1) AP configuration mode is only supported for Cyclone IV E devices.

Table 1–30 lists the JTAG timing parameters and values for Cyclone IV devices.

Table 1–30. JTAG Timing Parameters for Cyclone IV Devices (1)

Symbol	Parameter	Min	Max	Unit
t_{JCP}	TCK clock period	40	—	ns
t_{JCH}	TCK clock high time	19	—	ns
t_{JCL}	TCK clock low time	19	—	ns
t_{JPSU_TDI}	JTAG port setup time for TDI	1	—	ns
t_{JPSU_TMS}	JTAG port setup time for TMS	3	—	ns
t_{JPH}	JTAG port hold time	10	—	ns
t_{JPCO}	JTAG port clock to output (2), (3)	—	15	ns
t_{JPZX}	JTAG port high impedance to valid output (2), (3)	—	15	ns
t_{JPXZ}	JTAG port valid output to high impedance (2), (3)	—	15	ns
t_{JSSU}	Capture register setup time	5	—	ns
t_{JSH}	Capture register hold time	10	—	ns
t_{JSCO}	Update register clock to output	—	25	ns
t_{JSZX}	Update register high impedance to valid output	—	25	ns
t_{JSXZ}	Update register valid output to high impedance	—	25	ns

Notes to Table 1–30:

(1) For more information about JTAG waveforms, refer to "JTAG Waveform" in "Glossary" on page 1–37.

(2) The specification is shown for 3.3-, 3.0-, and 2.5-V LVTTL/LVCMOS operation of JTAG pins. For 1.8-V LVTTL/LVCMOS and 1.5-V LVCMOS, the output time specification is 16 ns.

(3) For EP4CGX22, EP4CGX30 (F324 and smaller package), EP4CGX110, and EP4CGX150 devices, the output time specification for 3.3-, 3.0-, and 2.5-V LVTTL/LVCMOS operation of JTAG pins is 16 ns. For 1.8-V LVTTL/LVCMOS and 1.5-V LVCMOS, the output time specification is 18 ns.

Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the high-speed I/O interface, external memory interface, and the PCI/PCI-X bus interface. I/Os using the SSTL-18 Class I termination standard can achieve up to the stated DDR2 SDRAM interfacing speeds. I/Os using general-purpose I/O standards such as 3.3-, 3.0-, 2.5-, 1.8-, or 1.5-LVTTL/LVCMOS are capable of a typical 200 MHz interfacing frequency with a 10 pF load.

For more information about the supported maximum clock rate, device and pin planning, IP implementation, and device termination, refer to *Section III: System Performance Specifications* of the *External Memory Interfaces Handbook*.

Actual achievable frequency depends on design- and system-specific factors. Perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specifications

Table 1–31 through Table 1–36 list the high-speed I/O timing for Cyclone IV devices. For definitions of high-speed timing specifications, refer to "Glossary" on page 1–37.

Table 1–31. RSDS Transmitter Timing Specifications for Cyclone IV Devices (1), (2), (4) (Part 1 of 2)

Symbol	Modes	C6			C7, I7			C8, A7			C8L, I8L			C9L			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	5	—	180	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×8	5	—	180	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×7	5	—	180	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×4	5	—	180	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×2	5	—	180	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×1	5	—	360	5	—	311	5	—	311	5	—	311	5	—	265	MHz
Device operation in Mbps	×10	100	—	360	100	—	311	100	—	311	100	—	311	100	—	265	Mbps
	×8	80	—	360	80	—	311	80	—	311	80	—	311	80	—	265	Mbps
	×7	70	—	360	70	—	311	70	—	311	70	—	311	70	—	265	Mbps
	×4	40	—	360	40	—	311	40	—	311	40	—	311	40	—	265	Mbps
	×2	20	—	360	20	—	311	20	—	311	20	—	311	20	—	265	Mbps
	×1	10	—	360	10	—	311	10	—	311	10	—	311	10	—	265	Mbps
t_{DUTY}	—	45	—	55	45	—	55	45	—	55	45	—	55	45	—	55	%
Transmitter channel-to-channel skew (TCCS)	—	—	—	200	—	—	200	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	—	—	—	500	—	—	500	—	—	550	—	—	600	—	—	700	ps
t_{RISE}	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	—	500	—	ps

Table 1–31. RSDS Transmitter Timing Specifications for Cyclone IV Devices (1), (2), (4) (Part 2 of 2)

Symbol	Modes	C6			C7, I7			C8, A7			C8L, I8L			C9L			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{LOCK} (3)	—	—	—	1	—	—	1	—	—	1	—	—	1	—	—	1	ms

Notes to Table 1–31:

(1) Applicable for true RSDS and emulated RSDS_E_3R transmitter.

(2) Cyclone IV E devices—true RSDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6. Emulated RSDS transmitter is supported at the output pin of all I/O Banks.
Cyclone IV GX devices—true RSDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated RSDS transmitter is supported at the output pin of I/O Banks 3, 4, 5, 6, 7, 8, and 9.

(3) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.

(4) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1–32. Emulated RSDS_E_1R Transmitter Timing Specifications for Cyclone IV Devices (1), (3) (Part 1 of 2)

Symbol	Modes	C6			C7, I7			C8, A7			C8L, I8L			C9L			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	5	—	85	5	—	85	5	—	85	5	—	85	5	—	72.5	MHz
	×8	5	—	85	5	—	85	5	—	85	5	—	85	5	—	72.5	MHz
	×7	5	—	85	5	—	85	5	—	85	5	—	85	5	—	72.5	MHz
	×4	5	—	85	5	—	85	5	—	85	5	—	85	5	—	72.5	MHz
	×2	5	—	85	5	—	85	5	—	85	5	—	85	5	—	72.5	MHz
	×1	5	—	170	5	—	170	5	—	170	5	—	170	5	—	145	MHz
Device operation in Mbps	×10	100	—	170	100	—	170	100	—	170	100	—	170	100	—	145	Mbps
	×8	80	—	170	80	—	170	80	—	170	80	—	170	80	—	145	Mbps
	×7	70	—	170	70	—	170	70	—	170	70	—	170	70	—	145	Mbps
	×4	40	—	170	40	—	170	40	—	170	40	—	170	40	—	145	Mbps
	×2	20	—	170	20	—	170	20	—	170	20	—	170	20	—	145	Mbps
	×1	10	—	170	10	—	170	10	—	170	10	—	170	10	—	145	Mbps
t_{DUTY}	—	45	—	55	45	—	55	45	—	55	45	—	55	45	—	55	%
TCCS	—	—	—	200	—	—	200	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	—	—	—	500	—	—	500	—	—	550	—	—	600	—	—	700	ps
t_{RISE}	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	—	500	—	ps

Table 1–32. Emulated RSDS_E_1R Transmitter Timing Specifications for Cyclone IV Devices (1), (3) (Part 2 of 2)

Symbol	Modes	C6			C7, I7			C8, A7			C8L, I8L			C9L			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{LOCK} (2)	—	—	—	1	—	—	1	—	—	1	—	—	1	—	—	1	ms

Notes to Table 1–32:

(1) Emulated RSDS_E_1R transmitter is supported at the output pin of all I/O Banks of Cyclone IV E devices and I/O Banks 3, 4, 5, 6, 7, 8, and 9 of Cyclone IV GX devices.

(2) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.

(3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1–33. Mini-LVDS Transmitter Timing Specifications for Cyclone IV Devices (1), (2), (4)

Symbol	Modes	C6			C7, I7			C8, A7			C8L, I8L			C9L			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK} (input clock frequency)	×10	5	—	200	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×8	5	—	200	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×7	5	—	200	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×4	5	—	200	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×2	5	—	200	5	—	155.5	5	—	155.5	5	—	155.5	5	—	132.5	MHz
	×1	5	—	400	5	—	311	5	—	311	5	—	311	5	—	265	MHz
Device operation in Mbps	×10	100	—	400	100	—	311	100	—	311	100	—	311	100	—	265	Mbps
	×8	80	—	400	80	—	311	80	—	311	80	—	311	80	—	265	Mbps
	×7	70	—	400	70	—	311	70	—	311	70	—	311	70	—	265	Mbps
	×4	40	—	400	40	—	311	40	—	311	40	—	311	40	—	265	Mbps
	×2	20	—	400	20	—	311	20	—	311	20	—	311	20	—	265	Mbps
	×1	10	—	400	10	—	311	10	—	311	10	—	311	10	—	265	Mbps
t_{DUTY}	—	45	—	55	45	—	55	45	—	55	45	—	55	45	—	55	%
TCCS	—	—	—	200	—	—	200	—	—	200	—	—	200	—	—	200	ps
Output jitter (peak to peak)	—	—	—	500	—	—	500	—	—	550	—	—	600	—	—	700	ps
t_{RISE}	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	—	500	—	ps
t_{FALL}	20 – 80%, C_{LOAD} = 5 pF	—	500	—	—	500	—	—	500	—	—	500	—	—	500	—	ps
t_{LOCK} (3)	—	—	—	1	—	—	1	—	—	1	—	—	1	—	—	1	ms

Notes to Table 1–33:

(1) Applicable for true and emulated mini-LVDS transmitter.

(2) Cyclone IV E—true mini-LVDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6. Emulated mini-LVDS transmitter is supported at the output pin of all I/O banks.
Cyclone IV GX—true mini-LVDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6. Emulated mini-LVDS transmitter is supported at the output pin of I/O Banks 3, 4, 5, 6, 7, 8, and 9.

(3) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.

(4) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1–34. True LVDS Transmitter Timing Specifications for Cyclone IV Devices (1), (3)

Symbol	Modes	C6		C7, I7		C8, A7		C8L, I8L		C9L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f_{HSCLK} (input clock frequency)	×10	5	420	5	370	5	320	5	320	5	250	MHz
	×8	5	420	5	370	5	320	5	320	5	250	MHz
	×7	5	420	5	370	5	320	5	320	5	250	MHz
	×4	5	420	5	370	5	320	5	320	5	250	MHz
	×2	5	420	5	370	5	320	5	320	5	250	MHz
	×1	5	420	5	402.5	5	402.5	5	362	5	265	MHz
HSIODR	×10	100	840	100	740	100	640	100	640	100	500	Mbps
	×8	80	840	80	740	80	640	80	640	80	500	Mbps
	×7	70	840	70	740	70	640	70	640	70	500	Mbps
	×4	40	840	40	740	40	640	40	640	40	500	Mbps
	×2	20	840	20	740	20	640	20	640	20	500	Mbps
	×1	10	420	10	402.5	10	402.5	10	362	10	265	Mbps
t_{DUTY}	—	45	55	45	55	45	55	45	55	45	55	%
TCCS	—	—	200	—	200	—	200	—	200	—	200	ps
Output jitter (peak to peak)	—	—	500	—	500	—	550	—	600	—	700	ps
t_{LOCK} (2)	—	—	1	—	1	—	1	—	1	—	1	ms

Notes to Table 1–34:

(1) Cyclone IV E—true LVDS transmitter is only supported at the output pin of Row I/O Banks 1, 2, 5, and 6.
Cyclone IV GX—true LVDS transmitter is only supported at the output pin of Row I/O Banks 5 and 6.

(2) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.

(3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1–35. Emulated LVDS Transmitter Timing Specifications for Cyclone IV Devices (1), (3) (Part 1 of 2)

Symbol	Modes	C6		C7, I7		C8, A7		C8L, I8L		C9L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f_{HSCLK} (input clock frequency)	×10	5	320	5	320	5	275	5	275	5	250	MHz
	×8	5	320	5	320	5	275	5	275	5	250	MHz
	×7	5	320	5	320	5	275	5	275	5	250	MHz
	×4	5	320	5	320	5	275	5	275	5	250	MHz
	×2	5	320	5	320	5	275	5	275	5	250	MHz
	×1	5	402.5	5	402.5	5	402.5	5	362	5	265	MHz
HSIODR	×10	100	640	100	640	100	550	100	550	100	500	Mbps
	×8	80	640	80	640	80	550	80	550	80	500	Mbps
	×7	70	640	70	640	70	550	70	550	70	500	Mbps
	×4	40	640	40	640	40	550	40	550	40	500	Mbps
	×2	20	640	20	640	20	550	20	550	20	500	Mbps
	×1	10	402.5	10	402.5	10	402.5	10	362	10	265	Mbps

Table 1–35. Emulated LVDS Transmitter Timing Specifications for Cyclone IV Devices (1), (3) (Part 2 of 2)

Symbol	Modes	C6		C7, I7		C8, A7		C8L, I8L		C9L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{DUTY}	—	45	55	45	55	45	55	45	55	45	55	%
TCCS	—	—	200	—	200	—	200	—	200	—	200	ps
Output jitter (peak to peak)	—	—	500	—	500	—	550	—	600	—	700	ps
t_{LOCK} (2)	—	—	1	—	1	—	1	—	1	—	1	ms

Notes to Table 1–35:

(1) Cyclone IV E—emulated LVDS transmitter is supported at the output pin of all I/O Banks.
Cyclone IV GX—emulated LVDS transmitter is supported at the output pin of I/O Banks 3, 4, 5, 6, 7, 8, and 9.

(2) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.

(3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

Table 1–36. LVDS Receiver Timing Specifications for Cyclone IV Devices (1), (3)

Symbol	Modes	C6		C7, I7		C8, A7		C8L, I8L		C9L		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f_{HSCLK} (input clock frequency)	×10	10	437.5	10	370	10	320	10	320	10	250	MHz
	×8	10	437.5	10	370	10	320	10	320	10	250	MHz
	×7	10	437.5	10	370	10	320	10	320	10	250	MHz
	×4	10	437.5	10	370	10	320	10	320	10	250	MHz
	×2	10	437.5	10	370	10	320	10	320	10	250	MHz
	×1	10	437.5	10	402.5	10	402.5	10	362	10	265	MHz
HSIODR	×10	100	875	100	740	100	640	100	640	100	500	Mbps
	×8	80	875	80	740	80	640	80	640	80	500	Mbps
	×7	70	875	70	740	70	640	70	640	70	500	Mbps
	×4	40	875	40	740	40	640	40	640	40	500	Mbps
	×2	20	875	20	740	20	640	20	640	20	500	Mbps
	×1	10	437.5	10	402.5	10	402.5	10	362	10	265	Mbps
SW	—	—	400	—	400	—	400	—	550	—	640	ps
Input jitter tolerance	—	—	500	—	500	—	550	—	600	—	700	ps
t_{LOCK} (2)	—	—	1	—	1	—	1	—	1	—	1	ms

Notes to Table 1–36:

(1) Cyclone IV E—LVDS receiver is supported at all I/O Banks.
Cyclone IV GX—LVDS receiver is supported at I/O Banks 3, 4, 5, 6, 7, 8, and 9.

(2) t_{LOCK} is the time required for the PLL to lock from the end-of-device configuration.

(3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

External Memory Interface Specifications

The external memory interfaces for Cyclone IV devices are auto-calibrating and easy to implement.

For more information about the supported maximum clock rate, device and pin planning, IP implementation, and device termination, refer to *Section III: System Performance Specifications* of the *External Memory Interface Handbook*.

Table 1–37 lists the memory output clock jitter specifications for Cyclone IV devices.

Table 1–37. Memory Output Clock Jitter Specifications for Cyclone IV Devices (1), (2)

Parameter	Symbol	Min	Max	Unit
Clock period jitter	$t_{JIT(per)}$	–125	125	ps
Cycle-to-cycle period jitter	$t_{JIT(cc)}$	–200	200	ps
Duty cycle jitter	$t_{JIT(duty)}$	–150	150	ps

Notes to Table 1–37:

(1) Memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2 standard.

(2) The clock jitter specification applies to memory output clock pins generated using DDIO circuits clocked by a PLL output routed on a global clock (GCLK) network.

Duty Cycle Distortion Specifications

Table 1–38 lists the worst case duty cycle distortion for Cyclone IV devices.

Table 1–38. Duty Cycle Distortion on Cyclone IV Devices I/O Pins (1), (2), (3)

Symbol	C6		C7, I7		C8, I8L, A7		C9L		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	45	55	%

Notes to Table 1–38:

(1) The duty cycle distortion specification applies to clock outputs from the PLLs, global clock tree, and IOE driving the dedicated and general purpose I/O pins.

(2) Cyclone IV devices meet the specified duty cycle distortion at the maximum output toggle rate for each combination of I/O standard and current strength.

(3) Cyclone IV E 1.0 V core voltage devices only support C8L, C9L, and I8L speed grades. Cyclone IV E 1.2 V core voltage devices only support C6, C7, C8, I7, and A7 speed grades. Cyclone IV GX devices only support C6, C7, C8, and I7 speed grades.

OCT Calibration Timing Specification

Table 1–39 lists the duration of calibration for series OCT with calibration at device power-up for Cyclone IV devices.

Table 1–39. Timing Specification for Series OCT with Calibration at Device Power-Up for Cyclone IV Devices (1)

Symbol	Description	Maximum	Units
t_{OCTCAL}	Duration of series OCT with calibration at device power-up	20	µs

Note to Table 1–39:

(1) OCT calibration takes place after device configuration and before entering user mode.

IOE Programmable Delay

Table 1–40 and Table 1–41 list the IOE programmable delay for Cyclone IV E 1.0 V core voltage devices.

Table 1–40. IOE Programmable Delay on Column Pins for Cyclone IV E 1.0 V Core Voltage Devices (1), (2)

Parameter	Paths Affected	Number of Setting	Min Offset	Max Offset					Unit
				Fast Corner		Slow Corner			
				C8L	I8L	C8L	C9L	I8L	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	2.054	1.924	3.387	4.017	3.411	ns
Input delay from pin to input register	Pad to I/O input register	8	0	2.010	1.875	3.341	4.252	3.367	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.641	0.631	1.111	1.377	1.124	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.971	0.931	1.684	2.298	1.684	ns

Notes to Table 1–40:

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–41. IOE Programmable Delay on Row Pins for Cyclone IV E 1.0 V Core Voltage Devices (1), (2)

Parameter	Paths Affected	Number of Setting	Min Offset	Max Offset					Unit
				Fast Corner		Slow Corner			
				C8L	I8L	C8L	C9L	I8L	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	2.057	1.921	3.389	4.146	3.412	ns
Input delay from pin to input register	Pad to I/O input register	8	0	2.059	1.919	3.420	4.374	3.441	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.670	0.623	1.160	1.420	1.168	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.960	0.919	1.656	2.258	1.656	ns

Notes to Table 1–41:

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–42 and Table 1–43 list the IOE programmable delay for Cyclone IV E 1.2 V core voltage devices.

Table 1–42. IOE Programmable Delay on Column Pins for Cyclone IV E 1.2 V Core Voltage Devices *(1), (2)*

Parameter	Paths Affected	Number of Setting	Min Offset	Max Offset								Unit
				Fast Corner			Slow Corner					
				C6	I7	A7	C6	C7	C8	I7	A7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.314	1.211	1.211	2.177	2.340	2.433	2.388	2.508	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.307	1.203	1.203	2.19	2.387	2.540	2.430	2.545	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.437	0.402	0.402	0.747	0.820	0.880	0.834	0.873	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.693	0.665	0.665	1.200	1.379	1.532	1.393	1.441	ns

Notes to Table 1–42:

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–43. IOE Programmable Delay on Row Pins for Cyclone IV E 1.2 V Core Voltage Devices *(1), (2)*

Parameter	Paths Affected	Number of Setting	Min Offset	Max Offset								Unit
				Fast Corner			Slow Corner					
				C6	I7	A7	C6	C7	C8	I7	A7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.314	1.209	1.209	2.201	2.386	2.510	2.429	2.548	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.312	1.207	1.207	2.202	2.402	2.558	2.447	2.557	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.458	0.419	0.419	0.783	0.861	0.924	0.875	0.915	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.686	0.657	0.657	1.185	1.360	1.506	1.376	1.422	ns

Notes to Table 1–43:

(1) The incremental values for the settings are generally linear. For the exact values for each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–44 and Table 1–45 list the IOE programmable delay for Cyclone IV GX devices.

Table 1–44. IOE Programmable Delay on Column Pins for Cyclone IV GX Devices *(1), (2)*

Parameter	Paths Affected	Number of Settings	Min Offset	Max Offset						Unit
				Fast Corner		Slow Corner				
				C6	I7	C6	C7	C8	I7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.313	1.209	2.184	2.336	2.451	2.387	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.312	1.208	2.200	2.399	2.554	2.446	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.438	0.404	0.751	0.825	0.886	0.839	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.713	0.682	1.228	1.41	1.566	1.424	ns

Notes to Table 1–44:

(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of the Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software.

Table 1–45. IOE Programmable Delay on Row Pins for Cyclone IV GX Devices *(1), (2)*

Parameter	Paths Affected	Number of Settings	Min Offset	Max Offset						Unit
				Fast Corner		Slow Corner				
				C6	I7	C6	C7	C8	I7	
Input delay from pin to internal cells	Pad to I/O dataout to core	7	0	1.314	1.210	2.209	2.398	2.526	2.443	ns
Input delay from pin to input register	Pad to I/O input register	8	0	1.313	1.208	2.205	2.406	2.563	2.450	ns
Delay from output register to output pin	I/O output register to pad	2	0	0.461	0.421	0.789	0.869	0.933	0.884	ns
Input delay from dual-purpose clock pin to fan-out destinations	Pad to global clock network	12	0	0.712	0.682	1.225	1.407	1.562	1.421	ns

Notes to Table 1–45:

(1) The incremental values for the settings are generally linear. For exact values of each setting, use the latest version of Quartus II software.

(2) The minimum and maximum offset timing numbers are in reference to setting **0** as available in the Quartus II software

I/O Timing

Use the following methods to determine I/O timing:

- the Excel-based I/O Timing
- the Quartus II timing analyzer

The Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get a timing budget estimation as part of the link timing analysis. The Quartus II timing analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after place-and-route is complete.

The Excel-based I/O Timing spreadsheet is downloadable from Cyclone IV Devices Literature website.

Glossary

Table 1–46 lists the glossary for this chapter.

Table 1–46. Glossary (Part 1 of 5)

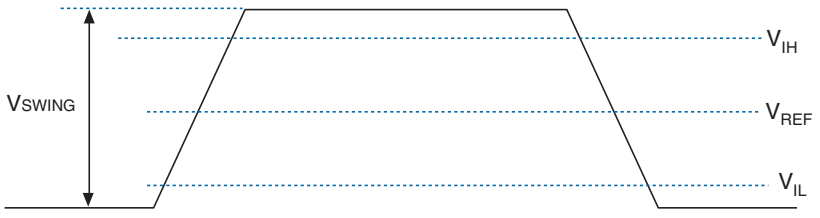
Letter	Term	Definitions
A	—	—
B	—	—
C	—	—
D	—	—
E	—	—
F	f_{HSCLK}	High-speed I/O block: High-speed receiver/transmitter input and output clock frequency.
G	GCLK	Input pin directly to Global Clock network.
	GCLK PLL	Input pin to Global Clock network through the PLL.
H	HSIODR	High-speed I/O block: Maximum/minimum LVDS data transfer rate (HSIODR = 1/TUI).
I	Input Waveforms for the SSTL Differential I/O Standard	

Table 1–46. Glossary (Part 2 of 5)

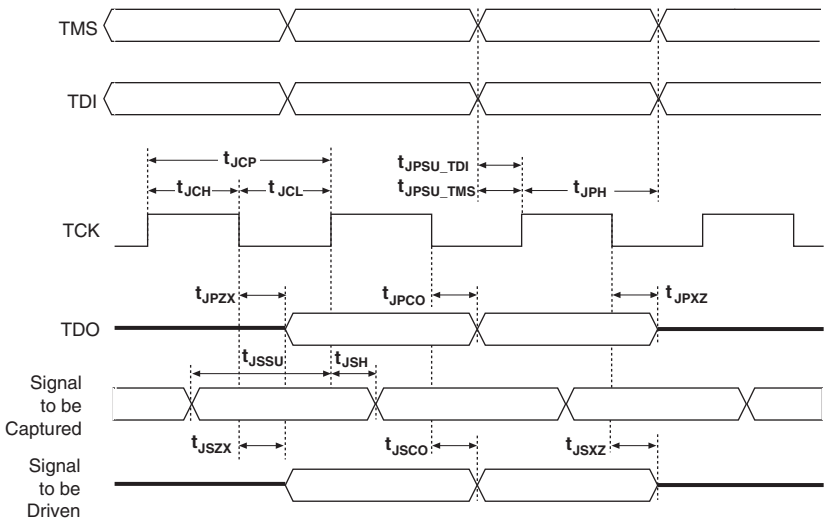
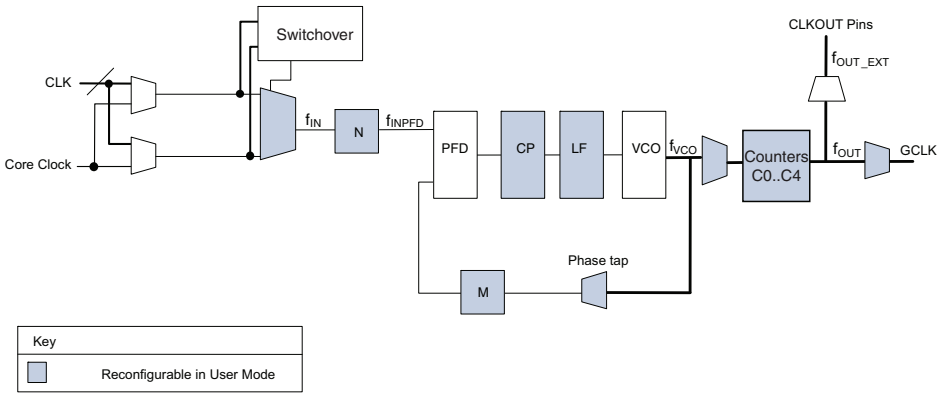
Letter	Term	Definitions
J	JTAG Waveform	
K	—	—
L	—	—
M	—	—
N	—	—
O	—	—
P	PLL Block	The following highlights the PLL specification parameters:
Q	—	—

Table 1–46. Glossary (Part 3 of 5)

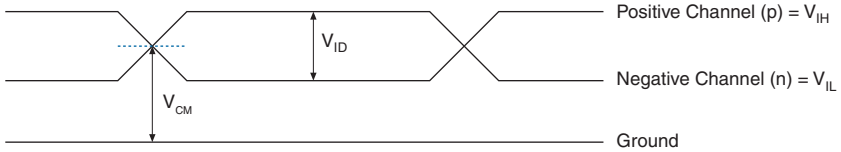
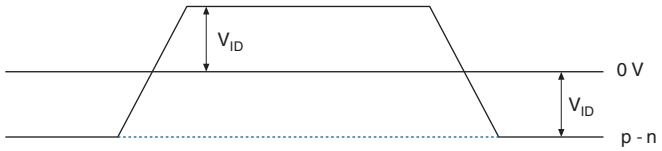
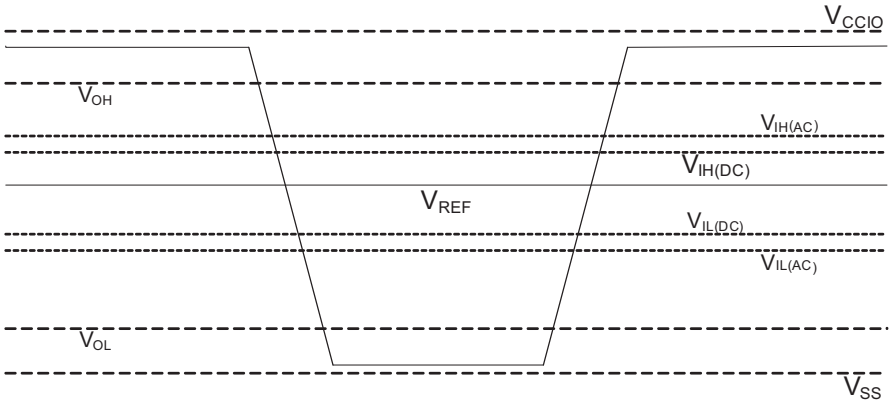
Letter	Term	Definitions
R	R_L	Receiver differential input discrete resistor (external to Cyclone IV devices).
	Receiver Input Waveform	Receiver input waveform for LVDS and LVPECL differential standards: **Single-Ended Waveform**  **Differential Waveform (Mathematical Function of Positive & Negative Channel)** 
	Receiver input skew margin (RSKM)	High-speed I/O block: The total margin left after accounting for the sampling window and TCCS. RSKM = (TUI – SW – TCCS) / 2.
S	Single-ended voltage-referenced I/O Standard	 The JEDEC standard for SSTI and HSTL I/O standards defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input crosses the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform *ringing*.
	SW (Sampling Window)	High-speed I/O block: The period of time during which the data must be valid to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window.

Table 1–46. Glossary (Part 4 of 5)

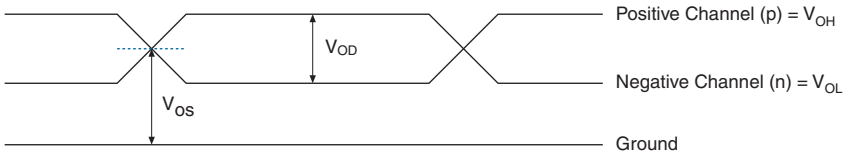
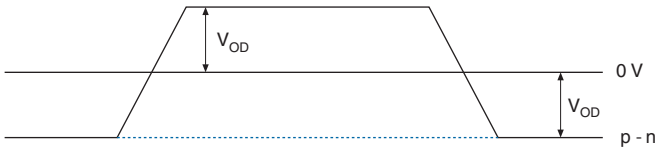
Letter	Term	Definitions
T	t_C	High-speed receiver and transmitter input and output clock period.
	Channel-to-channel-skew (TCCS)	High-speed I/O block: The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
	t_{cin}	Delay from the clock pad to the I/O input register.
	t_{CO}	Delay from the clock pad to the I/O output.
	t_{cout}	Delay from the clock pad to the I/O output register.
	t_{DUTY}	High-speed I/O block: Duty cycle on high-speed transmitter output clock.
	t_{FALL}	Signal high-to-low transition time (80–20%).
	t_H	Input register hold time.
	Timing Unit Interval (TUI)	High-speed I/O block: The timing budget allowed for skew, propagation delays, and data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w).
	$t_{INJITTER}$	Period jitter on the PLL clock input.
	$t_{OUTJITTER_DEDCLK}$	Period jitter on the dedicated clock output driven by a PLL.
	$t_{OUTJITTER_IO}$	Period jitter on the general purpose I/O driven by a PLL.
	t_{plicin}	Delay from the PLL inclk pad to the I/O input register.
	$t_{plicout}$	Delay from the PLL inclk pad to the I/O output register.
	Transmitter Output Waveform	Transmitter output waveforms for the LVDS, mini-LVDS, PPDS and RSDS Differential I/O Standards: **Single-Ended Waveform**  **Differential Waveform (Mathematical Function of Positive & Negative Channel)** 
	t_{RISE}	Signal low-to-high transition time (20–80%).
	t_{SU}	Input register setup time.
U	—	—

Table 1–46. Glossary (Part 5 of 5)

Letter	Term	Definitions
V	$V_{CM(DC)}$	DC common mode input voltage.
	$V_{DIF(AC)}$	AC differential input voltage: The minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential input voltage: The minimum DC input differential voltage required for switching.
	V_{ICM}	Input common mode voltage: The common mode of the differential signal at the receiver.
	V_{ID}	Input differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	V_{IH}	Voltage input high: The minimum positive voltage applied to the input that is accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage.
	$V_{IH(DC)}$	High-level DC input voltage.
	V_{IL}	Voltage input low: The maximum positive voltage applied to the input that is accepted by the device as a logic low.
	$V_{IL\ (AC)}$	Low-level AC input voltage.
	$V_{IL\ (DC)}$	Low-level DC input voltage.
	V_{IN}	DC input voltage.
	V_{OCM}	Output common mode voltage: The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential voltage swing: The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. $V_{OD} = V_{OH} – V_{OL}$.
	V_{OH}	Voltage output high: The maximum positive voltage from an output that the device considers is accepted as the minimum positive high level.
	V_{OL}	Voltage output low: The maximum positive voltage from an output that the device considers is accepted as the maximum positive low level.
	V_{OS}	Output offset voltage: $V_{OS} = (V_{OH} + V_{OL}) / 2$.
	$V_{OX\ (AC)}$	AC differential output cross point voltage: the voltage at which the differential output signals must cross.
	V_{REF}	Reference voltage for the SSTL and HSTL I/O standards.
	$V_{REF\ (AC)}$	AC input reference voltage for the SSTL and HSTL I/O standards. $V_{REF(AC)} = V_{REF(DC)}$ + noise. The peak-to-peak AC noise on V_{REF} must not exceed 2% of $V_{REF(DC)}$.
	$V_{REF\ (DC)}$	DC input reference voltage for the SSTL and HSTL I/O standards.
	$V_{SWING\ (AC)}$	AC differential input voltage: AC input differential voltage required for switching. For the SSTL differential I/O standard, refer to Input Waveforms.
	$V_{SWING\ (DC)}$	DC differential input voltage: DC input differential voltage required for switching. For the SSTL differential I/O standard, refer to Input Waveforms.
	V_{TT}	Termination voltage for the SSTL and HSTL I/O standards.
	$V_{X\ (AC)}$	AC differential input cross point voltage: The voltage at which the differential input signals must cross.
W	—	—
X	—	—
Y	—	—
Z	—	—

Document Revision History

Table 1–47 lists the revision history for this chapter.

Table 1–47. Document Revision History

Date	Version	Changes
December 2013	1.8	Updated Table 1–21 by adding Note (15).
May 2013	1.7	Updated Table 1–15 by adding Note (4).
October 2012	1.6	■ Updated the maximum value for V_I, V_{CCD_PLL}, V_{CCIO}, V_{CC_CLKIN}, V_{CCH_GXB}, and V_{CCA_GXB} Table 1–1. ■ Updated Table 1–11 and Table 1–22. ■ Updated Table 1–21 to include peak-to-peak differential input voltage for the Cyclone IV GX transceiver input reference clock. ■ Updated Table 1–29 to include the typical DCLK value. ■ Updated the minimum f_{HSCLK} value in Table 1–31, Table 1–32, Table 1–33, Table 1–34, and Table 1–35.
November 2011	1.5	■ Updated "Maximum Allowed Overshoot or Undershoot Voltage", "Operating Conditions", and "PLL Specifications" sections. ■ Updated Table 1–2, Table 1–3, Table 1–4, Table 1–5, Table 1–8, Table 1–9, Table 1–15, Table 1–18, Table 1–19, and Table 1–21. ■ Updated Figure 1–1.
December 2010	1.4	■ Updated for the Quartus II software version 10.1 release. ■ Updated Table 1–21 and Table 1–25. ■ Minor text edits.
July 2010	1.3	Updated for the Quartus II software version 10.0 release: ■ Updated Table 1–3, Table 1–4, Table 1–21, Table 1–25, Table 1–28, Table 1–30, Table 1–40, Table 1–41, Table 1–42, Table 1–43, Table 1–44, and Table 1–45. ■ Updated Figure 1–2 and Figure 1–3. ■ Removed SW Requirement and TCCS for Cyclone IV Devices tables. ■ Minor text edits.
March 2010	1.2	Updated to include automotive devices: ■ Updated the "Operating Conditions" and "PLL Specifications" sections. ■ Updated Table 1–1, Table 1–8, Table 1–9, Table 1–21, Table 1–26, Table 1–27, Table 1–31, Table 1–32, Table 1–33, Table 1–34, Table 1–35, Table 1–36, Table 1–37, Table 1–38, Table 1–40, Table 1–42, and Table 1–43. ■ Added Table 1–5 to include ESD for Cyclone IV devices GPIOs and HSSI I/Os. ■ Added Table 1–44 and Table 1–45 to include IOE programmable delay for Cyclone IV E 1.2 V core voltage devices. ■ Minor text edits.
February 2010	1.1	■ Updated Table 1–3 through Table 1–44 to include information for Cyclone IV E devices and Cyclone IV GX devices for Quartus II software version 9.1 SP1 release. ■ Minor text edits.
November 2009	1.0	Initial release.